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A front-end read out chip for the OPERA scintillator tracker

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Abstract

Multi-anode photomultipliers H7546 are used to readout signal from the OPERA Scintillator Tracker (CERN/SPSC 2000-028, SPSC/P318, LNGSP 25/2000; CERN/SPSC 2001-025, SPSC/M668, LNGS-EXP30/2001). A 32-channel front-end Read Out Chip prototype accommodating the H7546 has been designed at LAL. This device features a low-noise, variable gain preamplifier to correct for multi-anode non-uniformity, an auto-trigger capability 100% efficient at a 0.3 photo-electron, and a charge measurement extending over a large dynamic range [0–100] photo-electrons.

In this article we describe the ASIC architecture that is being implemented for the Target Tracker in OPERA, with a special emphasis put on the designs and the measured performance.

PACS: 84.30.−r; 84.30.Le; 84.30.Qi; 14.60.Pq

1. Overview of the OPERA experiment

1.1. The OPERA detector

The goal of the OPERA experiment, a massive lead/emulsion target, is to search for the appearance of $\nu_\mu \to \nu_\tau$ oscillations in the CNGS (CERN Neutrino to Gran Sasso) beam. It exploits nuclear emulsion for the unambiguous detection of the decay of the τ produced in ν_τ interactions. The detector is described in details in Ref. [1]. It is being built on the basis of two supermodules. Each supermodule consists of a target-tracker section where the interaction takes place followed by a muon spectrometer, allowing muon identification as well as sign and momentum determination. The target-tracker section is composed of 31 walls of 64×52 emulsion + lead bricks interpaced with scintillator tracker detector wall. These latter are used to identify the brick where the neutrino interaction took place for a precise scanning.

1.2. The scintillator target tracker

A complete detector description can be found in Ref. [1,2]. A scintillator wall consists of two scintillator planes, perpendicular to each other, and formed each by four 6.7 m length and 1.66 m wide modules, as shown in Fig. 1. A wall is used to provide both X and Y hit coordinates. Each module is made of 64 extruded scintillator strips, 6.7 m length, 1 cm thick, 2.6 cm wide of

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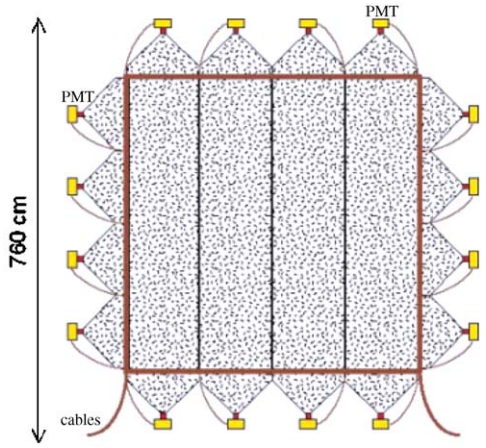

Fig. 1. A scintillator plane represented with the 64-channel PMTs used for the readout [1].

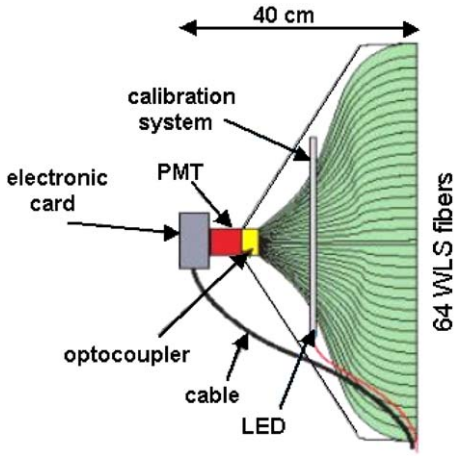

Fig. 2. Connection between a scintillator module and a 64-channel PMT [1] (see FN 1).

rectangular cross-section, which are obtained by extrusion with a TiO_2 co-extruded reflective coating for better light collection. Scintillator strips are designed with an embedded wavelength-shifting (WLS) fibre in the centre of the strip and readout at both ends. The selected strips are produced by AMCRYS Corp. [2]. The blue light emitted by each optically isolated strip is absorbed in the WLS fibre and re-emitted into the green, before a transmission to photomultiplier tubes (PMT) as sketched in Fig. 2. PMTs used by the experiment are 64-anodes ("pixels") PMT made by Hamamatsu[1] with a specific reference H8804MOD. As two PMTs are used to readout each module (at both ends), 16 PMTs are needed per scintillator wall, for a total of 992 PMTs for the full detector. A view of a multianode PMT is displayed in Fig. 3.

Covering a 2.3 mm × 2.3 mm area and formed by two series of 12 dynodes as sketched in Fig. 3, every PMT pixel is readout independently. For a nominal PMT supply voltage set between 800 and 900 V, individual pixel gains are ranged between 3×10^5 and 10^6 [3].

[1] Hamamatsu Photonics K.K., Electron Tube Center, 314-5, Shimokanzo, Toyooka-village, Iwata-gun, Shizuoka-ken, 438-0193, Japan.

1.3. Requirements on front-end electronics

The readout electronics of the Target Tracker is based on a 32-channel ASIC, referenced in the following as the OPERA Read Out Chip. Two such devices are used to readout each PMT for a total of 1984 chips for the full detector. Main requirements driving the chip design are the following: the chip must have a bandwidth large enough to match with a fast PMT pulse; it must correct for anode-to-anode gain variations; the ASIC must deliver a global auto-trigger as time information, with a 100% trigger efficiency for particles at minimum of ionization, corresponding to a few photoelectrons; and finally, it must deliver a charge proportional to the energy deposited in the scintillator for a charge ranging between 1 and 100 photoelectrons.

PMT pixel-to-pixel gain variation have been measured with a specific test bench described in Ref. [3]. Fig. 4 displays the signal output gain as measured along the X and Y pixels of a 64-anodes PMT illuminated by an LED, while Fig. 5 shows the gain as function of pixel number. Pixel-to-pixel variations by a factor as large as three are seen among the channels of the same PMT. In order to compensate for this large difference between channels, the front-end electronics will be equipped with an adjustable gain system, directly incorporated in the preamplifier stage. This allows

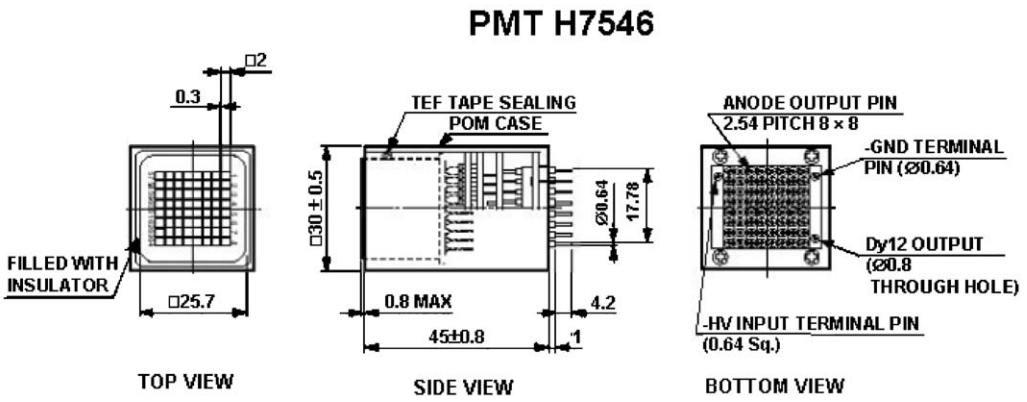

Fig. 3. The Hamamatsu H7546 PMT [2].

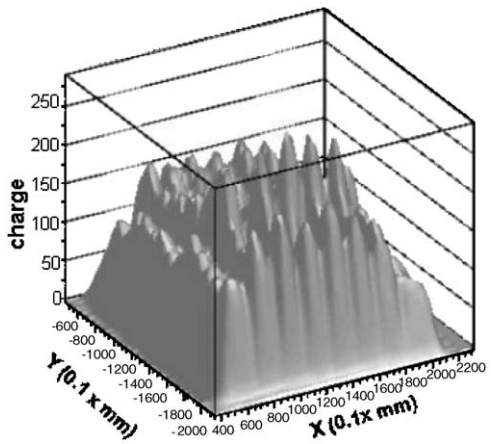

Fig. 4. Gain variations as seen for the 64 channels of the H7546 PMT by Hamamatsu [3].

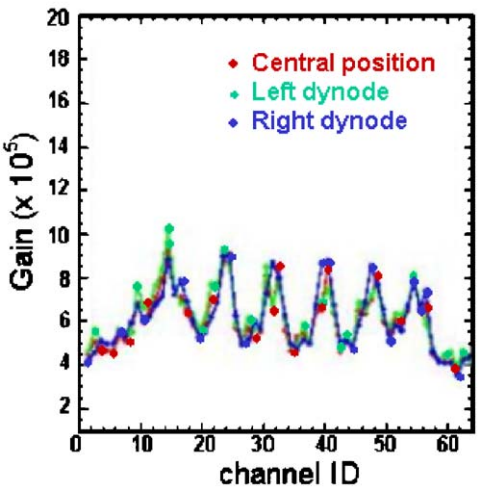

Fig. 5. Gain variations as seen for the 64 channels of the H7546 PMT by Hamamatsu [3].

good integration density and delivers a signal of identical range to the trigger and charge measurement arms of every channel.

The auto-trigger stage has been designed to be a low noise, 100% efficient in the detection of particles at minimum of ionization (MIP), corresponding to about 6 p.e.'s for muons traversing the scintillator at the centre of the strips.

Fig. 6 shows the light yield as function of the distance from the impact to the PMT. This distance is ranging from a few cm to 7.6 m with a fibre attenuation length typically above 700 cm. These characteristics impose strong requirements on the trigger capabilities, and a 100% trigger efficiency is required as low as a $\frac{1}{3}$rd of photoelectron, which corresponds to about 50 fC at the anode for a PMT gain of 10^6.

Finally, a dynamic range of the charge measurement up to about 100 photoelectrons is required, which corresponds to 16 pC at a gain of 10^6. This should allow to distinguish MIP from particle showers, and provide a measurement of the energy deposition in EM showers relevant for the event classification. The charge measurement must of course be effective for any individual (preamplifier) gain correction.

2. Main features of the ASIC

The Read-Out chip is a 32-channel ASIC with individual input, trigger and charge measurement. The ASIC produces a multiplexed output for the 32 individual charge measurements as well as a hit register, signalling all triggered channels.

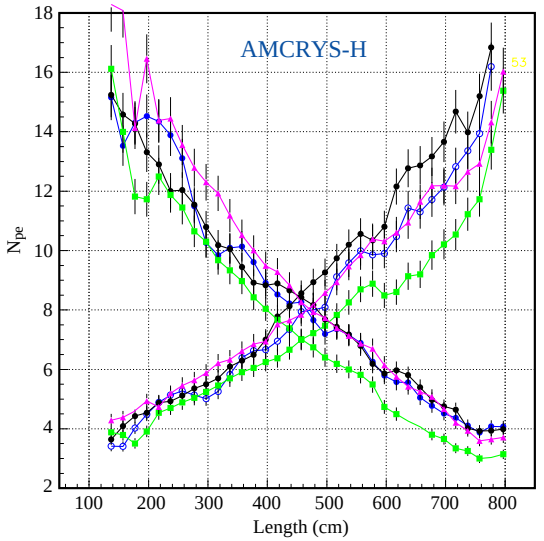

Fig. 6. Light yields at both ends of a scintillator strip module for different choices of scintillator fibres. In all cases, an MIP corresponds to more than six photoelectrons [2].

2.1. Single-channel architecture

The architecture of one channel is presented in Fig. 7 as a block functionality diagram; a detailed description of the signal path is displayed in Fig. 8.

The ASIC comprises a low noise, low impedance variable gain preamplifier that feeds both a trigger and a charge measurement part. The gain correction functionality makes use of a current mirror structure that is set via a series of switches to amplify the input signal up to a factor 3.5.

The trigger channel includes a fast shaper followed by a low offset comparator, whose threshold voltage is common for all channels. A trigger decision is formed by the logical "OR" of all 32 comparator outputs, which is used for generating an external Hold signal for the charge measurement part. A mask register allows at this stage to disable any noisy or malfunctioning channel.

The charge measurement arm consists of a slow shaper followed by a Sample & Hold buffer. Upon a trigger decision, charges are stored in 2 pF capacitors and the 32 channels outputs are readout sequentially at a 5 MHz frequency, in a period of time of 6.4 μs.

2.2. ASIC global architecture

The technology of the chip is AMS BiCMOS 0.8 μm [5]. The chip area is about 10 mm^2 and it is packaged in a QFP100 case. The chip

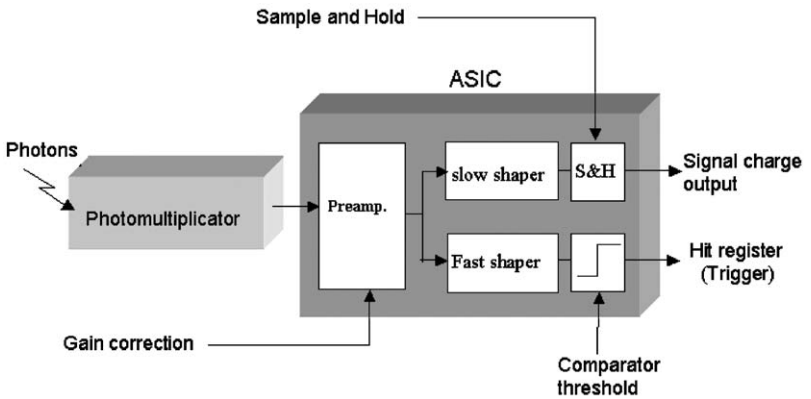

Fig. 7. Block schematics of a single channel architecture.

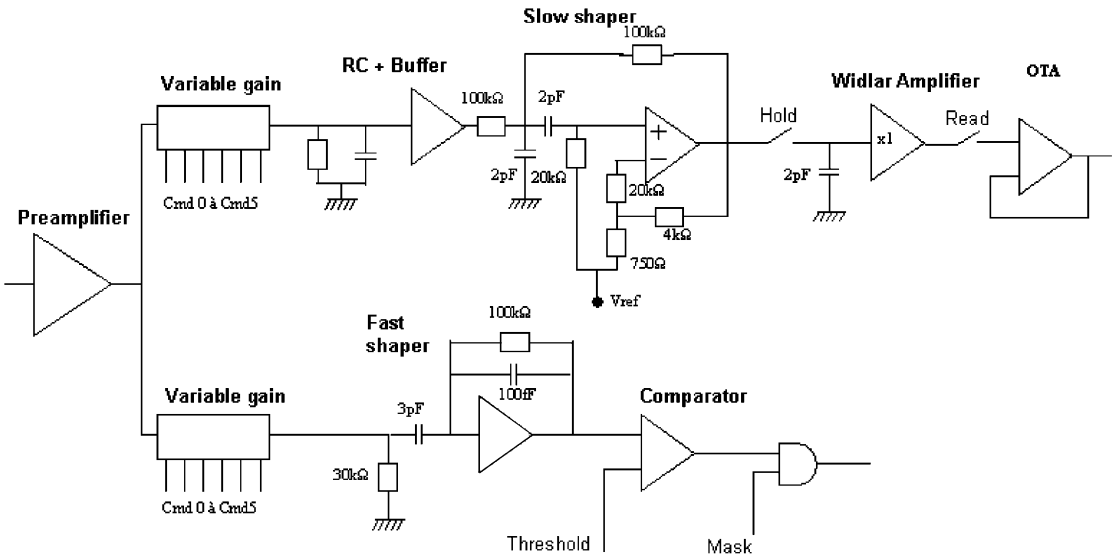

Fig. 8. Schematics of a single-channel architecture.

consumption depends upon the gain correction settings and is ranging between 130 and 160 mW total. The complete chip comprises 32 channels and 2 extra test channels that are designed to provide reference voltages for the trigger and for the charge measurement.

3. Variable gain preamplifier

3.1. Preamplifier architecture

The variable gain preamplifier is built around current mirror and switches preceded by a current conveyor. The preamplifier input stage is designed around a "super common base" architecture, whose schematics is shown in Fig. 9. With this architecture, the input impedance is set to a reasonably low value of about 100 Ω while keeping small currents circulating in the mirror, and thereby reducing cross-talk.

The common base used as current conveyor is mounted in the feedback loop of a simple amplifier, R_C allowing to obtain low input impedance with small bias currents in Q_2 and the following mirrors. The simple conveyor input impedance $Z_{in} = 1/g_{m2}$ thus becomes

$$\frac{R_0 + 1/g_{m2}}{1 + g_{m1}R_c}.$$

This closed-loop architecture strongly decreases the input impedance by $(1 + g_{m1}R_c) \approx 30$. The input impedance can be controlled by the bias current of Q_1 as $g_{m1} = I_{c1}/V_T$ and is set to about 100 Ω to minimize cross-talk and sensitivity to the detector capacitance. For the fast channel, the signal goes directly in the fast shaper. It can be noted that the input impedance starts increasing past 10 MHz, then referred to as "inductive behaviour" which can lead to oscillation with a capacitive detector. Integrated technology with careful transistor dimensioning allows to overcome this effect.

3.2. Current mirrors

Two copies of the input current are made available, one for the fast channel to obtain the time information of the particle interaction with the detector, and the other for the slow channel to measure the charge. For the slow channel, the current which goes out from the mirror is

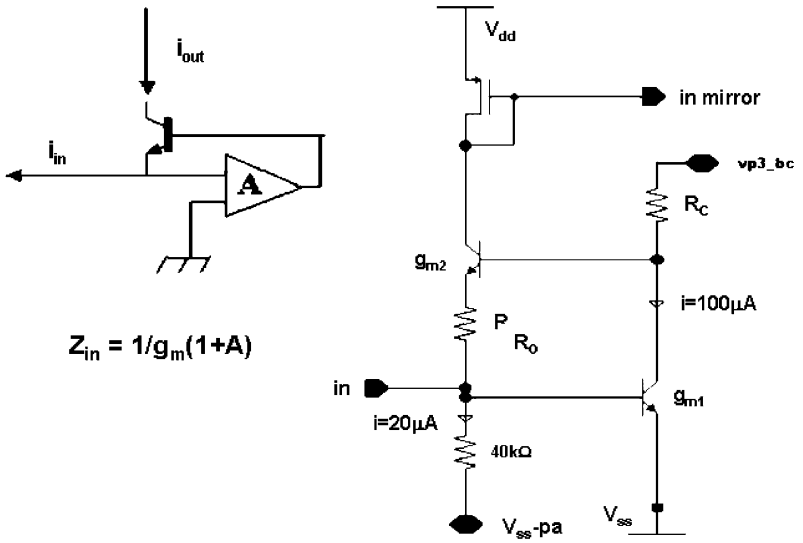

Fig. 9. Super common base preamplifier architecture.

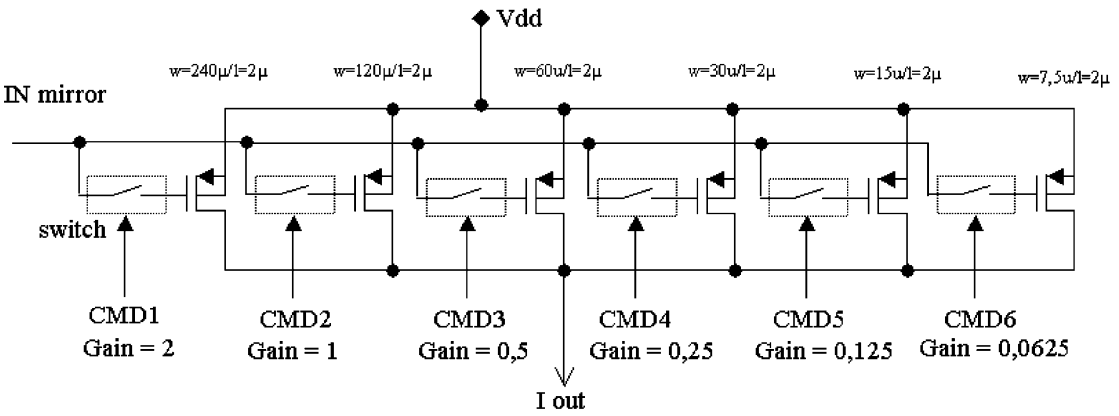

Fig. 10. Schematics of the current mirror architecture.

converted into a voltage signal in an RC cell ($R = 30\ \mathrm{k\Omega}$ and $C = 10$ pF). The global transfer function is given by: $V_{\mathrm{out}}/I_{\mathrm{in}} = -R/(1 + sRC)$ with $\tau = RC = 300$ ns. The gain amplification functionality makes use of switchable current mirrors with various areas (2, 1, 0.5, 0.25, 0.125, 0.0625), which allows amplification factors ranging from 0 to a theoretical value of 3.94 times the input signal. By turning off all current switches any channel can also be disabled externally, thanks to its null gain in its input stage. Schematics of the mirror's architecture is shown in Fig. 10.

3.3. Preamplifier performance

Preamplifier gain is measured on the RC integrating cell and found to be 94 mV/pC (15 mV/p.e. at gain 10^6) with a rise time (10–90%) of about 30 ns, for a correction gain set to 1. All current mirror branches have been tested and found reliable. The corresponding 6 switches allow to set 64 amplification levels of correction per channel, ranging from 0, where the channel is disabled, to a 3.55 times the input. Fig. 11 shows the measured performance on a single channel.

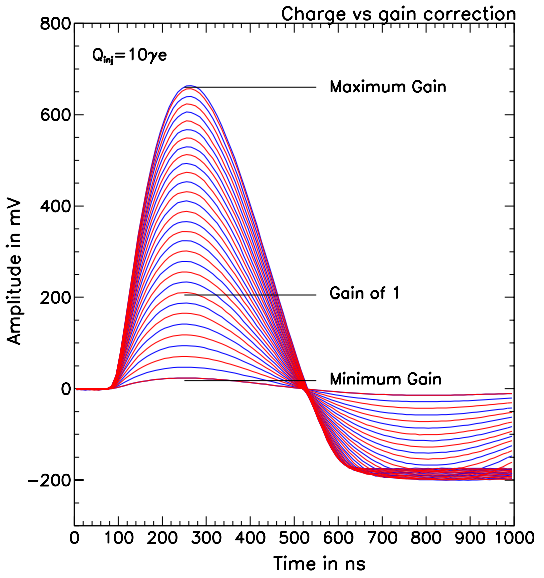

Fig. 11. Slow shaper output wave-forms for a 10 p.e. input charge for 32 levels of preamplifier amplification.

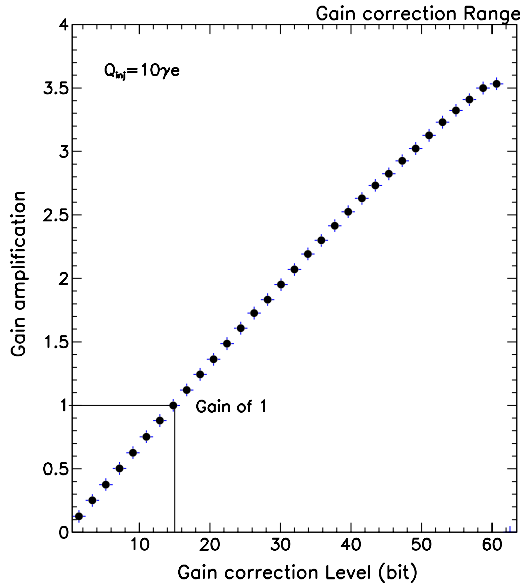

Fig. 12. Effective gain amplification as function of the preamplifier level settings for a single channel.

The one-to-one correspondance between the bit correction level and the effective gain is displayed in Fig. 12, which shows that the maximal effective gain that can be reached is 3.55 as all current mirrors are added.

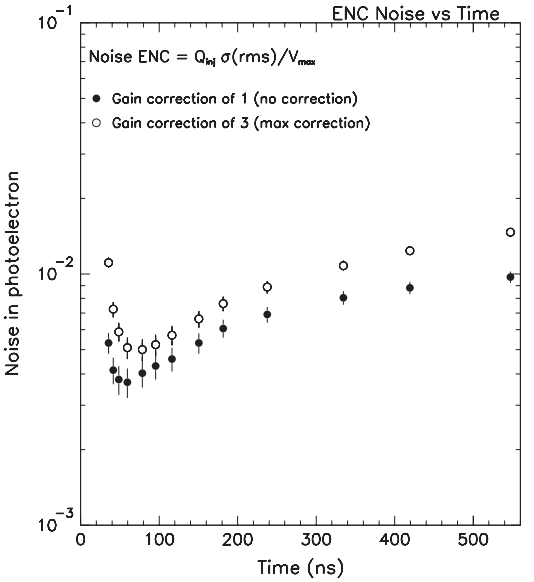

Fig. 13. Noise RMS in photoelectron at the preamplifier output stage as function of shaping time constant.

Equivalent noise charge (ENC) at the preamplifier output has been measured as function of shaping time constant, and is displayed in Fig. 13. For a timing corresponding to both the fast (10 ns) and slow shaping times (200 ns), the noise RMS is found at or below 1% of photoelectron, which is not expected to affect the trigger nor the charge measurement capabilities.

4. Trigger channel

4.1. Fast shaper architecture

The fast shaper is directly fed with the mirror output via a 3 pF capacitance and is integrated in a 0.1 pF charge amplifier. The time constant of integration is set to 10 ns to produce a fast signal and a differential input is used to minimize offset dispersion and allow a common threshold for the chip with a minimal spread. The simulated open-loop performances are shown in Fig. 14. The open-loop gain is $G_0 = 220$, with a gain bandwidth product GBW = 220 MHz and a dominant pole at

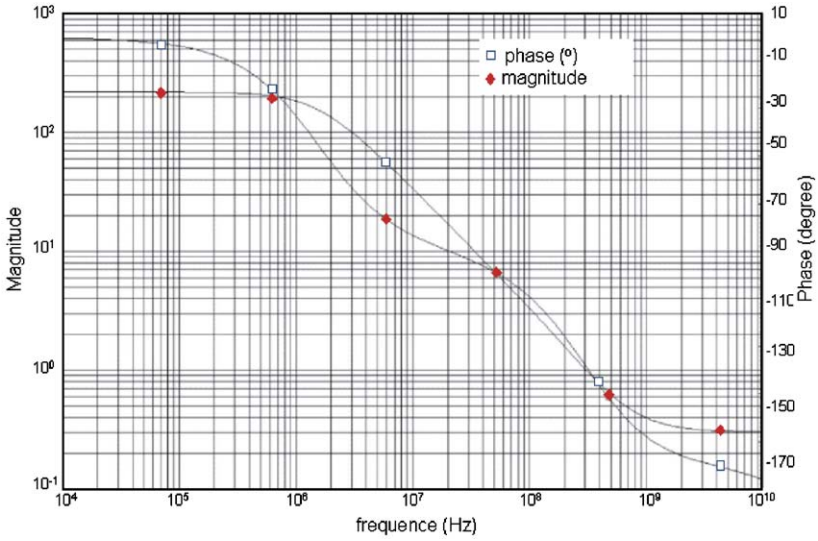

Fig. 14. Simulated fast shaper open-loop performance. Top curve shows the phase variation with frequency (right scale). Bottom curve shows the magnitude (left scale).

$W_0 = 1$ MHz. The phase margin is about 40°. Thus a 1 p.e. signal produces a 400 mV pulse easy to discriminate.

4.2. Comparator architecture

The comparator input stage is designed with a bipolar differential pair in order to minimize the offset. With a low offset comparator and a high gain in the preceeding shaping a common low-dispersion threshold can be used for all channels. A 1 trigger decision is taken if at least one of the 32 fast shaper channels detects a signal above the threshold, which is set by one external voltage for all 32 channels. A (trigger) mask register has been added in order to disable any selected channel.

4.3. Fast shaper and comparator performance

The fast shaper is characterized by a gain of 2.5 V/pC, i.e. 400 mV/p.e., with a peaking time of 10 ns for a preamplifier gain set to 1. The gain becomes 6.0 V/pC for a maximal preamplifier gain settings, which corresponds to 270 mV/p.e., assuming that the gain correction factor of 3.55 is used for correctly compensating the gain spread of the PMTs for the charge measurement.

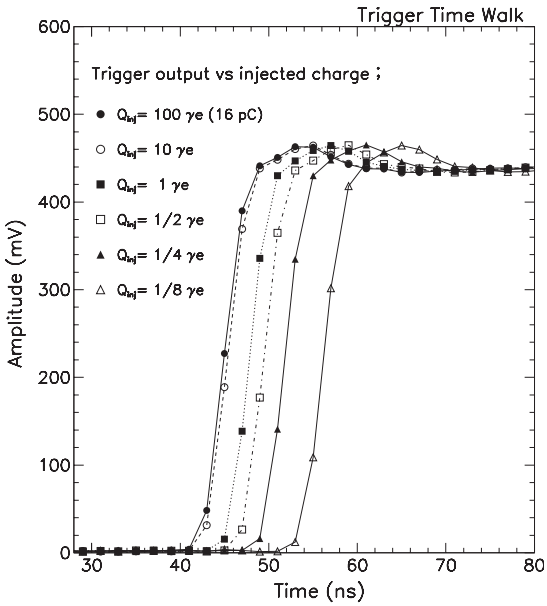

Fig. 15. Trigger response for input charges ranging between 100 and 1/8 p.e. with a trigger threshold of 0.1 p.e.

The output signal from the comparator is a 5 V signal which is then converted to a 450 mV pseudo-LVDS signal, as shown in Fig. 15. In this figure is also shown the trigger comparator outputs as function of the time, for input charges

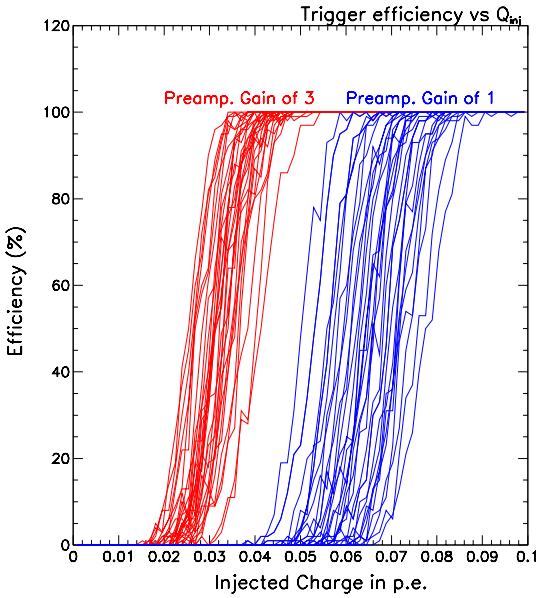

Fig. 16. Trigger efficiency (S-curve) as function of the input charge for the 32 channels for a preamplifier gains of 1 and 3.

corresponding to 0.125, 0.25, 0.5, 1, 10 and 100 p.e. From these results it appears that the trigger rise-time only slightly depends on the injected charge magnitude, since an increase from 0.1 to 100 p.e. in the input signal only results in a 15 ns delay in the trigger decision. This delay is not expected to affect significantly the charge measurement precision, since a ± 10 ns variation of the sampling time only corresponds to a relative change of a few $\frac{1}{1000}$ in the charge sampling. Regarding the time measurement, and given the attenuation factor in the 6-m-long scintillators, this delay is again not expected to play any significant role, since no precise time measurement is needed on the scintillator ends.

The trigger efficiency has been measured as a function of the input charge for each individual channel. Characteristic S-shaped curves obtained for gain = 1 and 3 are displayed in Fig. 16 for all 32 channels of a chip. For gain = 1 a trigger efficiency of 100% is found for all channels and for an injected charge as small as 0.1 p.e., which fulfills the requirements set by the collaboration at 0.3 p.e. The threshold spread for the 32 channels is around 0.03 p.e., which implies an offset spread of ± 5 mV. For gain = 3 the S-curves moved toward lower charge values as expected. The slight deviation from the expected factor 3 is interpreted as a small dependence of the fast shaper risetime on the gain.

The noise at the fast shaper output can be measured directly using the intermediate outputs of a test channel located on the same chip or it can be indirectly extracted from the S-curves using the slope at the 50% trigger efficiency point. Direct measurements lead to a noise RMS of about 1.0 mV found for gain = 1 (i.e., 400 mV/p.e.) and 3.3 mV for gain = 3.55, in agreement with indirect determination, which corresponds to 0.005 and 0.012 p.e., respectively.

5. Charge measurement channel

5.1. Slow shaper architecture

The mirror output is made available as a voltage pulse on the RC integrator and is shaped by a CRRC shaper with a time constant set to minimize the sensitivity to the arrival time. The shaper is included in a Sallen–Key structure. In order to minimize pedestal variation from channel-to-channel slow shaper DC offset dispersion, again a differential input stage has been used. To reduce the offset, the amplifier has a bipolar NPN differential pair on its input stage. The design of this stage makes a centroid as symmetric as possible and a PMOS transistor was added on the non-inverting side. The slow shaper open-loop transfer function is shown in Fig. 17. The amplifier is characterized by a gain band width product GBW = 720 MHz, an open-loop gain $G_0 = 720$ and a dominant pole at $W_0 = 1$ MHz.

5.2. Sample & Hold structure

The slow shaper is followed by a Sample & Hold system and a multiplexed output. The maximum of the slow shaper output signal is stored in a 2 pF capacitance. When a trigger signal occurs, all the capacitors are read sequentially through a shift register made by D-flip-flop.

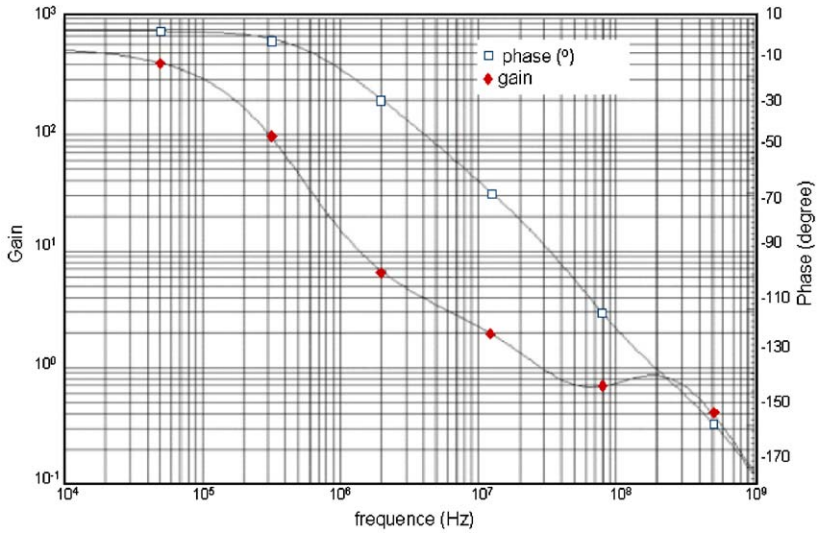

Fig. 17. Simulated slow shaper open-loop transfer function. Top curve shows the phase variation with frequency (right scale). Bottom curve shows the magnitude (left scale).

In order to fully benefit from such improvement in the charge measurement, the Sample & Hold architecture has been improved and a buffer structure using a Widlar differential configuration has been implemented. NMOS transistors are used to avoid leakage current. Fig. 18 shows the Widlar configuration of the Sample & Hold buffer.

5.3. Charge measurement performance

Fig. 19 displays the waveform output of a single channel for input charges ranging from 1 to 100 photoelectrons with a preamplifier gain set to 1. The full response range is set from a few mV corresponding to a fraction of photoelectron to 2.0 V for a 100 p.e. input charge.

For a preamplifier gain set to 1, the average gain of the slow shaper is 121 ± 1 mV/pC equivalent to 19.0 ± 0.2 mV/p.e. Results are quite stable among channels since channel-to-channel variations show an RMS of 1.2% (gain = 1) and 1.5% (gain = 3.55). The average peaking time with respect to the input signal is 163 ns for a 10 p.e. input charge, with a corresponding rise time of 160 ns, with a maximal spread among the 32 channels of ± 4 ns. Peaking time is shown to depend slightly upon the input charge, and goes down by about 5 ns as the input charge is increased from 1 to 100 p.e., as shown in Fig. 20. We also measure a slight dependence of the peaking time upon the

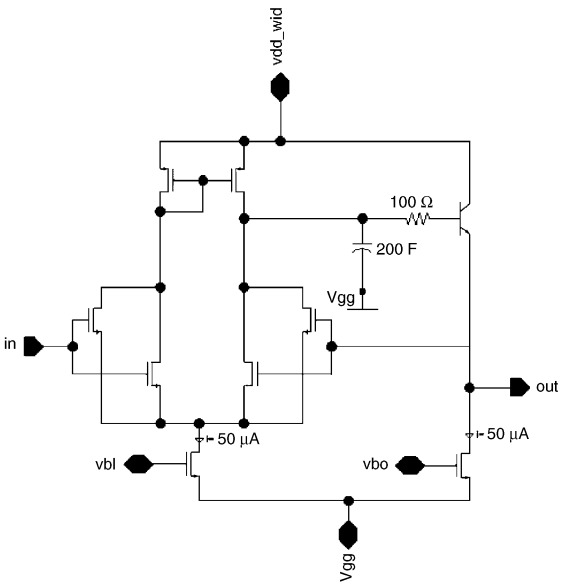

Fig. 18. Widlar configuration of the Sample & Hold system.

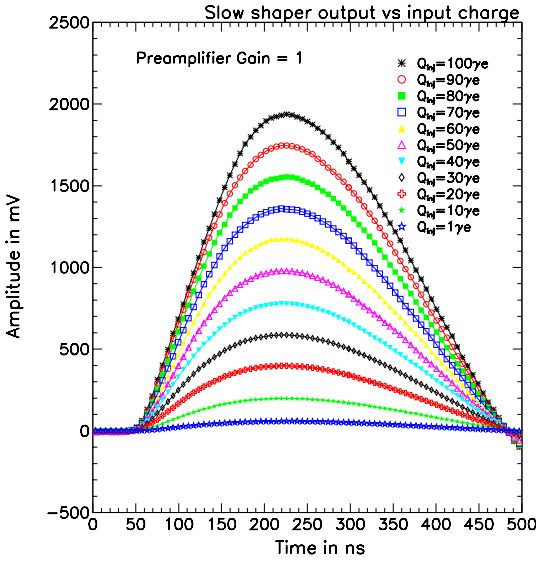

Fig. 19. Slow shaper waveform outputs for different input charge corresponding to 1–100 p.e.

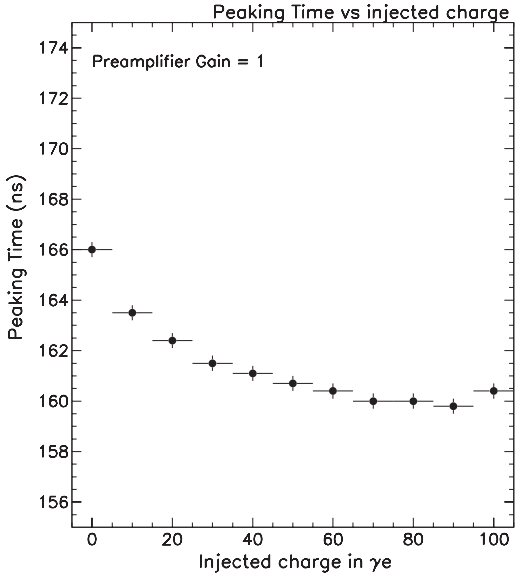

Fig. 20. Peaking Time as function of the injected charge for a single channel with a preamplifier gain of 1.

preamplifier gain, with a 15 ns increase as one sets the preamplifier gain from 1 to 3.55.

The choice of a relatively long time constant is justified by the need to avoid any significant

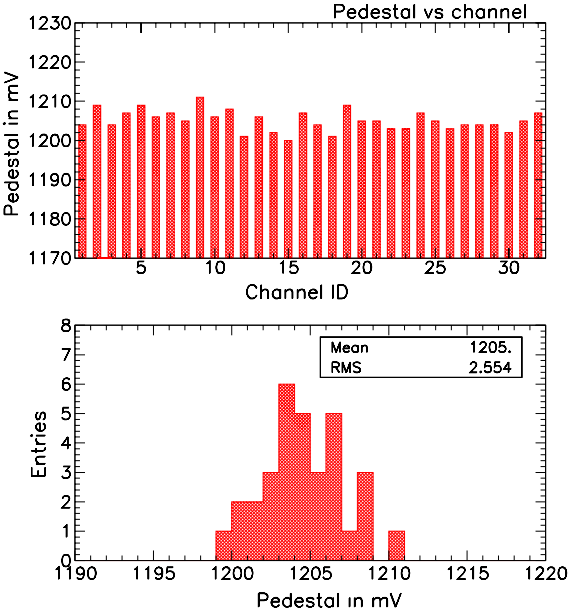

Fig. 21. Pedestal as measured for all 32 channels of the chip (top), and pedestal mean value distribution (bottom).

variation on the charge measurement in a sampling window of ± 10 ns. Indeed, within this time window, no difference exceeding 0.5% is seen in the maximal waveform voltage. This choice makes the chip rather unsensitive to the magnitude of the input charge as well as to trigger time delay.

The average quiescent voltage of the 32 channels is about 1.2 V, with a spread of ± 6 mV (Fig. 21). This corresponds to less than a 0.3 p.e. pedestal spread for the charge output. Note that, on the OPERA readout board, the signal actually digitized by the ADC is the difference between the multiplexed output and the Channel 0 output. This channel is not connected to any input, and using its output as a reference makes the measurements insensitive to pedestal variations common to all channels (temperature effect, etc.).

5.4. Linearity of the charge measurement

The linearity in the charge measurement has been assessed for all channels as function of an input charge ranging between 1 and 100 p.e. It

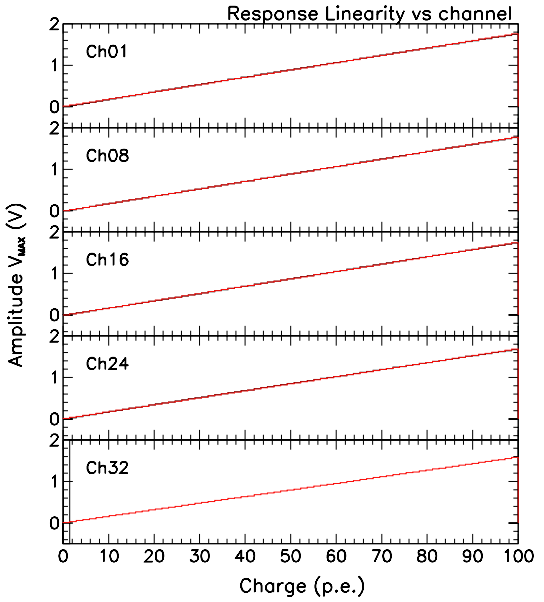

Fig. 22. Response linearity in the charge measurement as function of the input injected charge for five channels.

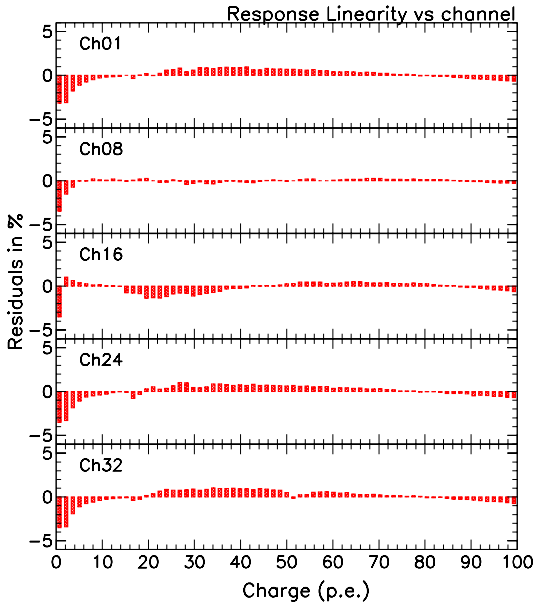

Fig. 23. Response linearity residuals as function of the injected

has been checked for different values of gain correction.

Fig. 22 displays the readout charge for channels 1, 8, 16, 24 and 32 as a function of the injected

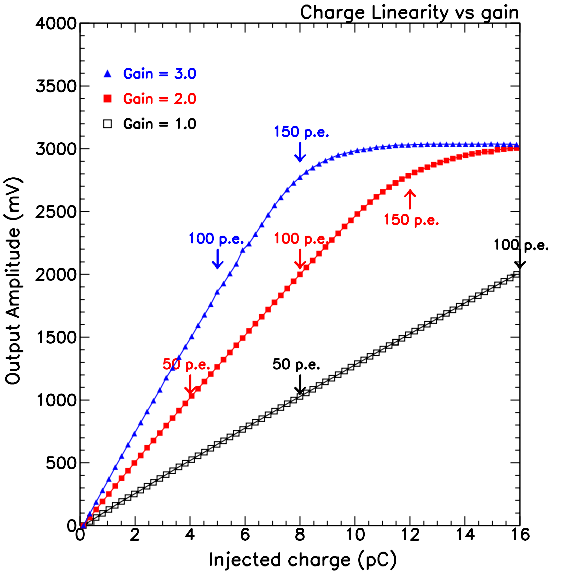

Fig. 24. Linearity of the charge measurement as function of the input charge for a gain set at 1, 2, and 3.5. Note that a photoelectron corresponds to 160 Fc at gain 1, 80 Fc at gain 2, and 53 Fc at a gain of 3.

charge, and compares it with the results of a linear fit, while Fig. 23 shows the residuals computed as the difference between measurement and the fit. No deviation above 2% is seen over the full [1–100] photoelectrons range. The dynamic range could be further extended by increasing the supply voltage from the present setting of 5 V. Indeed the choice of the AMS BiCMOS technology [4] makes it possible to set this value up to 6 V with no degradation of the performance.

The dynamic range naturally depends upon the preamplifier gain settings. Fig. 24 shows the effects of increasing the gain setting of a single channel from a gain of 1, where 1 p.e. is equivalent to 160 fC, to a maximal effective gain of 3.55, where 1 p.e. corresponds to 40 fC. Linearity is found to be quite unsensitive to the gain settings, with a dynamic range extending above 100 p.e. in all cases.

5.5. Electronic cross-talk

Physical cross-talk between adjacent pixels is known to be non-negligible for the multi-anode

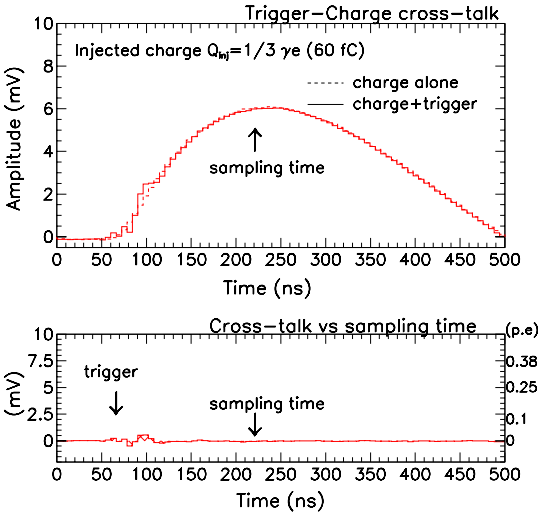

Fig. 25. Effects on a charge channel due to the trigger-charge coupling. Top plot shows the output waveforms with (dashed) and without (plain) a trigger decision as a function of the time. Bottom plot shows the difference of the two waveforms as a function of the time.

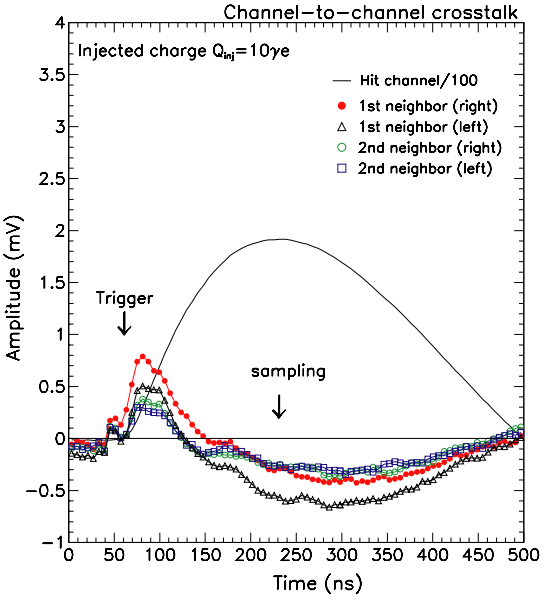

Fig. 26. Signal output for a channel with an injected charge of 10 p.e. (plain line, divided by 100 on the display) as a function of the time compared to the cross-talk induced charge in the 1st and 2nd neighbouring channels on each side of the hit channel.

PMTs, with effects that can be as high as 2–3% between two adjacent channels. This sets a reference value with which we have to compare electronic sources of cross-talks induced in the ASIC itself.

Two kinds of cross-talks are found to affect the charge measurement of any individual channel: a first source is due to a coupling between the trigger and the charge measurement arm, which causes a slight distortion of the charge signal upon a trigger decision; a second effect is seen between neighbouring channels, where a large charge in a single channel can induce a signal in a locally close track.

Trigger-charge couplings can cause the distortion of the signal waveform. This effect is illustrated in Fig. 25, which shows the signal output waveform used to measure the charge, and compares it to the very same waveform obtained upon a trigger decision. It appears that the digital signal (0–2 V logic) output from the comparator produces a glitch that can be seen on the corresponding channel. However, while this effect is sizeable around the time at which the trigger decision occurs, its magnitude at the sampling time is less than 0.1%, which is considered as negligible.

On the ASIC, couplings between tracks that are close to each other may also cause a signal to be seen in several neighbouring channels. Fig. 26 displays the output signal for a single channel with an injected charge of 10 photoelectrons, and compares it with the charge outputs observed in the 1st, 2nd and 3rd neighbouring channels. It is shown that the charge induced by cross-talk has a negative sign and a magnitude of the order of 0.1–0.25% of the input charge at the sampling time.

At earlier times the effect is maximal in the 1st neighbour, as expected, but never completely vanishes, whatever the channel location may be. This implies that there are two contributions to the cross-talk: the first being due to capacitive couplings at the inputs, which effects mainly the 1st neighbouring channels to the one with the injected charge, and the second effecting equally all the channels, on a level up to 0.7% of the input

charge for some of the tested chips, and which is due to an internal, not well understood coupling. This cross-talk can be easily eliminated by using the difference of the signals at the multiplexer output and the channel 0 output, because channel 0 shows the same effect like all other channels. Using this differential signal, the level of cross-talk in the first neighbouring channel is at most 0.2% at the sampling time. This holds for "realistic signals" coming from the PMT anode with a typical width of 5–10 ns. A possible explanation for this phenomenon is the saturation of the preamplifier for sharp input signal.

For the full dynamic range, we thus quote conservatively a cross-talk of 0.5% and conclude that no significant effect is expected from the ASIC itself. We note that during physics use, cross-talk in non-neighbouring channels is negligible since the multiplexer output is channel 0 baseline subtracted. This technic will be used for the OPERA Target Tracker [5] readout to reduce effects common to all channels.

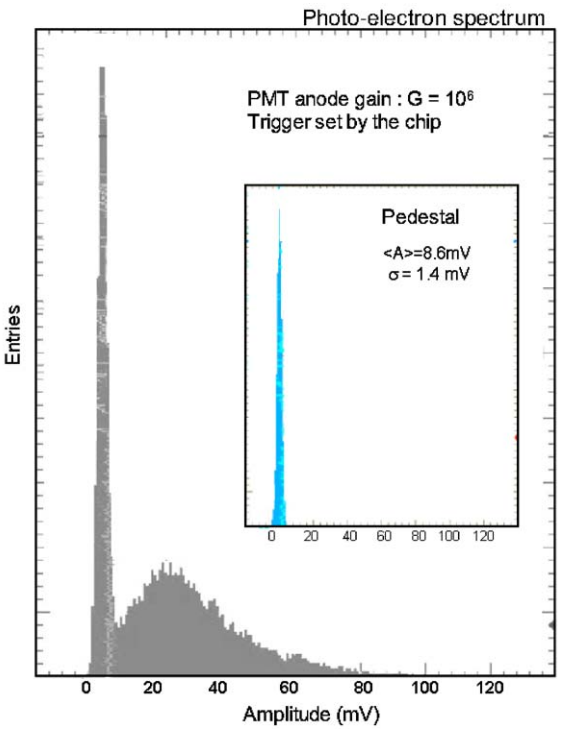

Fig. 27. Pulse height distribution of PMT signals induced by weak LED pulses, which produce one photoelectron in average. The LED signal illuminates 8 non-neighbouring channels of the multi-anode PMT. The response of only one channel is shown. The ASIC produces a trigger if the signal of at least one channel exceeds the threshold, which was set to 0.015 p.e.

6. PMT readout with the ASIC

A multianode PMT has been used to test the ASIC response to a photoelectron signal. An analog board equipped with 2 ASICs has been designed, assembled and connected to the 64 anode PMT. A set of LEDs have been used to illuminate 8 fibres simultaneously inside a black box.

The trigger signal provided by the ASIC, defined as the logical OR of all 32 channels, allows to record the pulse height distribution of any channel. Fig. 27 shows the pulse height distribution obtained for weak LED pulses, which produce one photoelectron in average. This spectrum contains 38% of events with no photoelectron, which produce the sharp pedestal peak.

7. Summary of performance

Table 1 reports the performance as measured on the 32 channel chip. The FE electronic ASIC designed and tested by both LAL and Bern Group is found to satisfy the OPERA Target Tracker requirements: the preamplifier stage allows to correct for the gain differences of the individual PMT channels up to a factor 3.5 with a good precision; the auto-trigger functionality has been tested and found to be 100% efficient at 0.3 p.e. signal level and with a negligible electronic noise; the charge measurement works well with less than 1% channel-to-channel cross-talk and a dynamic range of about 125 p.e. with a good linearity (1%) up to 100 p.e.

The 2000 ASICs produced for the OPERA Target Tracker are now in the process of being installed in the analog boards. Scintillator walls and the associated front-end electronics are

Table 1
Performance of the OPERA Read Out chip

Preamplifier:	
Gain correction	Range 0–3.5 (6-bit resolution)
Input for test pulse	3 pF alternate (even/odd channels)
Input impedance	$Z_{in} \approx 100\ \Omega$
Auto-trigger:	
Fast shaper peak time	10 ns
Fast shaper gain (Gain 1)	2.5 V/pC (400 mV/p.e.)
Threshold spread (peak-to-peak)	± 0.015 p.e.
Fast shaper noise (Gain 1)	1.8 mV (0.72 fC or 0.005 p.e.)
Trigger sensitivity	100% at 0.3 p.e.
Hit register	Implemented
Charge measurement:	
Dynamic range (Gain 1)	16 pC (100 p.e.)
Slow shaper peak time (Gain 1)	160 ns
Slow shaper gain (Gain 1)	120 mV/pC (19 mV/p.e.)
Pedestal spread (mV) (peak-to-peak)	± 6 mV (± 0.4 p.e.)
Noise @ MUX rms (Gain 1)	1.3 mV (12 fC or 0.075 p.e.)
Cross-talk	$O(0.5\%)$
Linear voltage range at MUX	about 1.2–3.2 V
Readout frequency	5 MHz (6.4 μs/32ch.)

currently being produced for a detector completion expected in 2006.

One can notice that other experimental fields make use of the ASICs developed initially for the OPERA experiment. These are projects in imaging technologies in biomedical sciences, for X-rays radioscopy dosimetry [6] as well as for γ-camera used in positron tomography [7].

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