The OPERA ROC: a front-end Read Out Chip for the OPERA Scintillator Tracker

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Abstract

Multi-anode photomultipliers HM7546 are used to readout signal from the OPERA Scintillator Tracker [1]. A 32-channels front-end read out chip (ROC) prototype accomodating the HM7546 has been designed at LAL. This device features a low-noise, variable gain preamplifier to correct for multi-anode non-uniformity, an auto-trigger capability 100% efficient at a 1/4th of a photo-electron, and a charge measurement extending over a large dynamic range between [0-100] photo-electrons. Procedures have been defined and applied to the ASIC in view of its validation for physics use. Results show that the present front-end ROC fully satisfies the Target Tracker requirements. Proposal is to consider the present ASIC as the baseline readout chip for the Target Tracker.

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1 Introduction

1.1 The OPERA experiment

The goal of the OPERA experiment, a massive lead/emulsion target, is to search for the appearance of $\nu_\mu \rightarrow \nu_\tau$ oscillations in the CNGS (Cern Neutrino to Gran Sasso) beam. It exploits nuclear emulsion for the unambiguous detection of the decay of the τ produced in ν_τ interactions. The detector is displayed in Fig. 1.1 and is being built on the basis of two supermodules. Each supermodule consists of a target-tracker section where the interaction takes place followed by a muon spectrometer, allowing muon identification as well as sign and momentum determination. The target-tracker section is composed of 31 walls of emulsion+lead bricks interpaced with scintillator tracker detector wall. These latter are used to identify the brick where the neutrino interaction took place for a precise scanning.

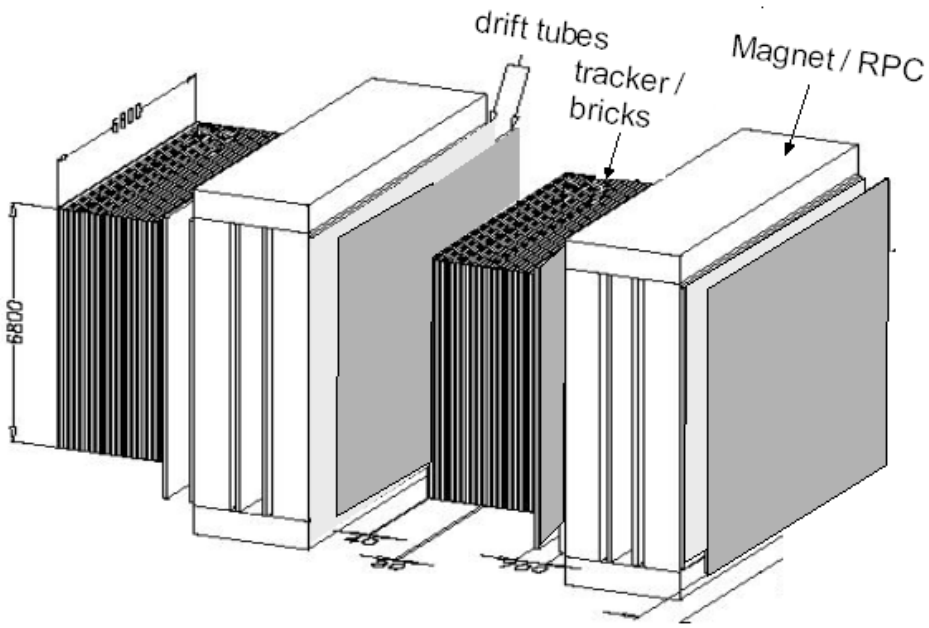

Figure 1.1: *View of the Opera detector*

1.2 The scintillator target tracker

A scintillator wall consists of two scintillator planes, perpendicular to each other, and formed each by four 6.7 m length and 1.66 m wide modules, as shown in Fig. 1.2. A wall is used to provide both the X and Y hit coordinates. Each module is made of 64 extruded scintillator strips, 6.7 m length, 1 cm thick, 2.6 cm wide of rectangular cross-section, which are obtained by extrusion with a TiO_2 co-extruted reflective coating for better light collection. Scintillator strips are designed with an embedded wavelength-shifting (WLS) fiber in the center of the strip

and readout at both ends. The blue light emitted by each optically isolated strip is absorbed in the WLS fiber and re-emitted into the green, before a transmission to photomultiplier tubes (PMT) as sketched in Fig. 1.3. PMTs used by the experiment are 64-anodes ("pixels") PMT made by Hamamatsu and referrenced as H8804MOD. As two PMTs are used to readout each module (at both ends), 16 PMTs are needed per scintillator wall, for a total of 992 PMTs for the full detector.

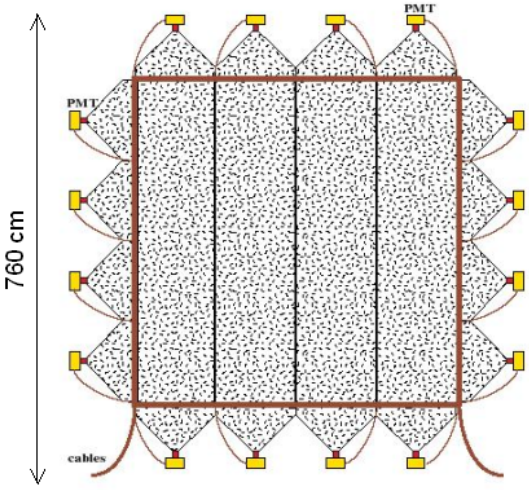

Figure 1.2: *A scintillator plane represented with the 64-channel PMT's used for the readout*

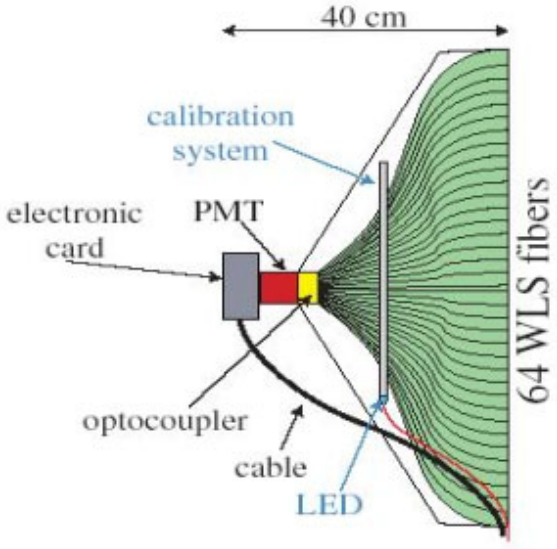

Figure 1.3: *Connection between scintillator module and a 64-channel PMT*

Each of the 64 PMT pixel, covering a 2.3 mm $\times$ 2.3 mm^2 area and formed by two series of 12 dynodes, is readout independentely. For a nominal PMT supply voltage taken between 800 and 900 V, individual gain is ranging between 3×10^5 and 10^6. It has to be noticed that pixel gain may vary from channel to channel by a factor as large as 3 [4]. Detector details can be found in Ref. [2].

Nb of units	per plane	per wall	for the full detector
Scintillator modules	4	8	496
Scintillator strips	256	512	31,744
PMT's	8	16	992
FE Readout ASIC	16	32	1,984

Table 1: *Summary of the main numbers for the Target electronic tracker*

1.3 Requirements on front-end electronics

The readout electronics of each Target Tracker is based on a 32-channel ASIC, referrenced in the following as the OPERA Read Out Chip. Two such devices are used to readout each PMT for a total of 1,984 chips for the full detector. Main requirements driving the chip design are the following: the chip has to have a large bandwidth necessary for a good matching with a fast PMT signal shape; the chip must correct the signal for anode-to-anode gain variations; the ASIC must deliver a global auto-trigger as time information, with a 100% trigger efficiency for particles at minimum of ionization (MIP); finally, the chip must deliver a charge proportional to the energy deposited in the scintillator for a charge ranging between 1 and 100 photoelectrons.

PMT pixel-to-pixel gain variation have been measured with a specific test bench described in Ref [4]. Fig. 1.4 displays the signal output gain as measured along the X and Y pixels of a 64-anodes PMT for a fixed input charge, while Fig. 1.5 shows the gain as function of pixel number. Pixel-to-pixel variations by a factor as large as 3 are seen among the channels of the same PMT. In order to compensate this large difference between channels, the front-end electronics must be equipped with an adjustable gain system, directly incorporated in the preamplifier stage. This allows good integration density and delivers a signal of identical range to the fast and slow shaper of every channel.

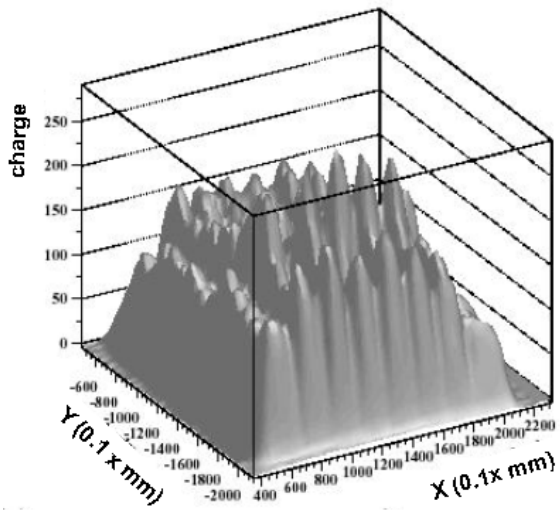

Figure 1.4: *Gain variations as seen for the 64 channels of the H7546 PMT by Hamamatsu*

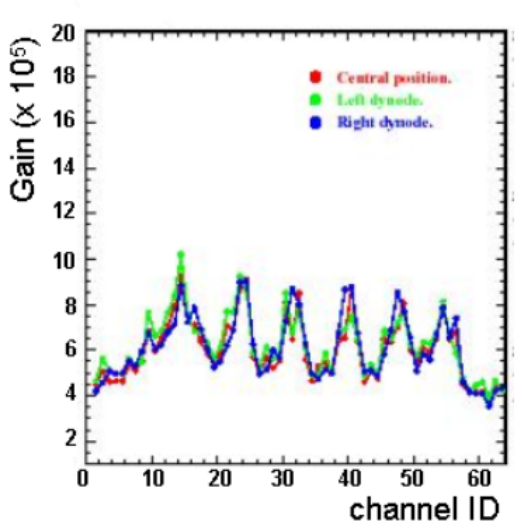

Figure 1.5: *Gain variations as seen for the 64 channels of the H7546 PMT by Hamamatsu*

The auto-trigger stage has been designed to be a low noise, 100% efficient in the detection of particles at minimum of ionsation (MIP). Typically, particles traversing the scintillator at the center of the strips, deposit around 6 photo-electrons. Fig. 1.6 shows the light yield as function of the distance from the impact to the PMT. This distance is ranging from a few cm to 7.6 m

with a fiber attenuation length typically above 700 cm. These characteristics impose strong requirements on the trigger capabilities, and a 100% trigger efficiency is required as low as a 1/3rd of photoelectron, which corresponds to about 50 fC at the anode for a PMT gain of 10^6. Besides, we aim at a front end approaching a signal to noise ratio of 100 for 1 p.e. signal, which would allow an auto-trigger at a level of 1/16 p.e, much lower than the 100% trigger efficiency for a 1/3rd photoelectrons signal required for the OPERA experiment.

Finally, a dynamic range of the charge measurement up to about 100 photoelectrons is required, which corresponds to 16 pC at a gain of 10^6. This should allow to distinguish MIP from particle showers, and provide a measurement of the energy deposition in EM showers relevant for the event classification. The charge measurement must of course be effective for any individual (preamplifier) gain corrections ranging from 1 to 3.

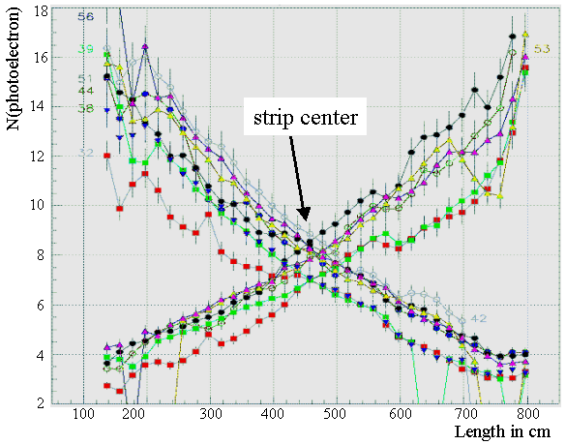

Figure 1.6: *Light yields at both ends of a scintillator strip module for different choices of scintillator fibers. In all cases, a MIP corresponds to more than 6 photoelectrons*

The LAL shares the responsability with Bern University to provide the front end electronics for the 992 PMT's (that is 1,984 chips) used to readout signals from the scintillator Target Tracker of OPERA. While LAL designs the ASIC's used to readout signal from the scintillator Target Tracker, Bern university designs the mother Boards that is implemented on the FE chip.

2 Design of the OPERA Read Out Chip (ROC)

The chip comprises 32 front-end channels with individual inputs, trigger and charge measurement. Each channel includes a variable gain, based on a current mirror architecture; an auto-trigger channel including a fast shaper (t_p = 10 ns) followed by a comparator; and a charge measurement channel, with a slow shaper (t_p = 200 ns) and a track and hold structure. The charge is stored in a 2 pF capacitance and the 32 channels outputs are multiplexed. The logical "OR" of all the comparator outputs gives the trigger ; the threshold is global for the 32 channels and a mask register allows to disable a noisy channel. A schematics of single channel is displayed on Fig. 2.7.

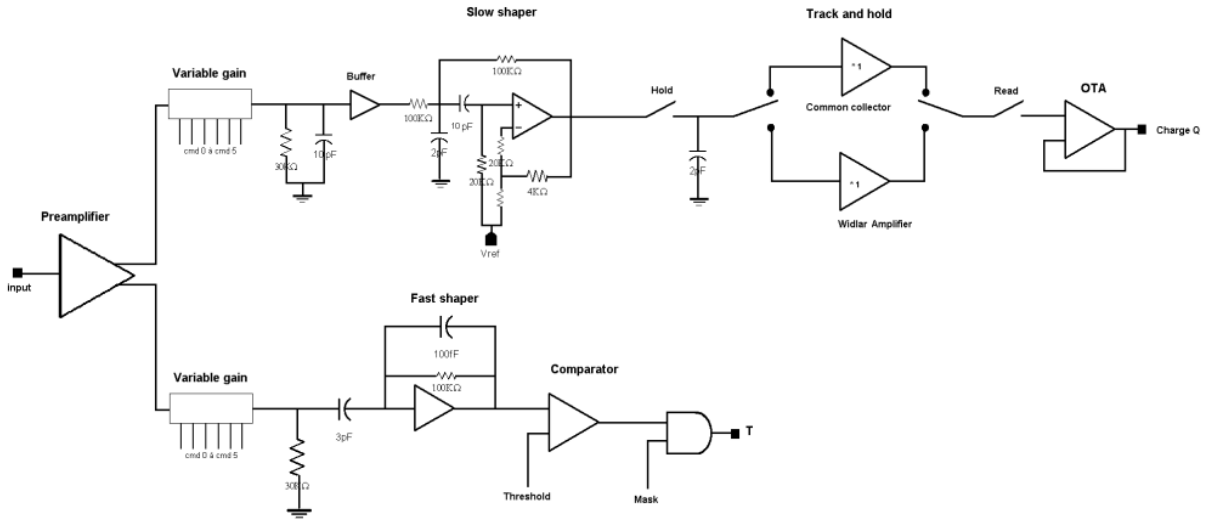

Figure 2.7: *Architecture of a single channel*

The technology of this chip is AMS BiCMOS 0.8μm [5]. The chip area is about 10 mm^2 and it is packaged in a QFP100 case. The consumption is about 185 mW and is shown to vary very little around this value. The layout and the pin-out of the chip are presented in Fig. B.44 in Appendix B.

2.1 Preamplifier architecture

The ASIC preamplifier is low-noise, variable gain preamplifier device. The variable gain system is implemented by adding switchable current mirrors with various areas (2, 1, 0.5, 0.25, 0.125, 0.0625), which allows a gain correction from 0 to about 3,94. By turning off all current switches any channel can be disabled externally, thanks to its null gain in its input stage. This functionnality makes the trigger mask register a redundant feature. The input impedance of a simple current mirror as used in version-2 [8] is too large even at 100 μA bias current and with wide transistors, so a current conveyor (Q_2) on the input has been added. Moreover, a feedback

amplifier (with a simple common emitter (Q_1) architecture) has been implemented to improve and control the input impedance value. So, this chip includes a new input amplifier stage which has been designed around a super common base. Schematics represented in Fig. 2.8 shows the principle of the preamplifier.

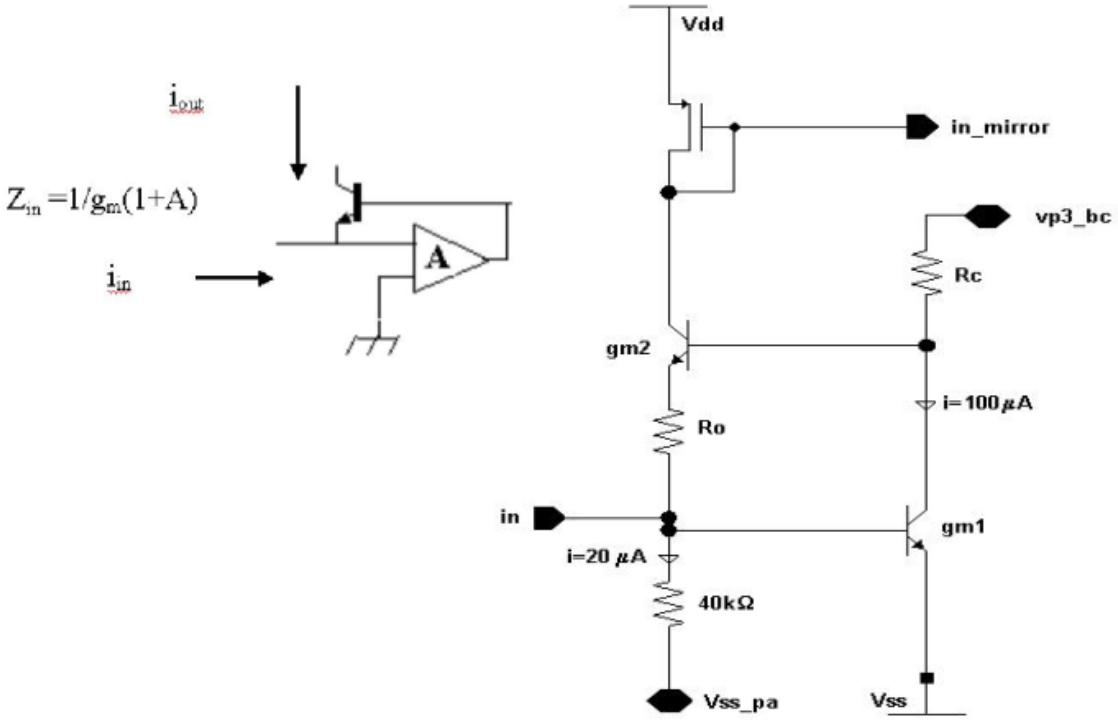

Figure 2.8: *ROC Preamplifier Architecture*

With this architecture, the simple conveyor input impedance $Z_{in} = 1/g_{m2}$ becomes:

$$\frac{R_0 + 1/g_{m2}}{1 + g_{m1}R_c}$$

This closed loop architecture strongly decreases the input impedance by $(1+g_{m1}R_c) \approx 30$, so, the current in the mirror can be divided by 5 (from 100μA to 20μA) compared to version-2 and the transistor width can be decreased while keeping a reasonable input impedance in the vicinity of 100 Ω. The input impedance can be controlled by the bias current of Q_1 as $g_{m1} = I_{c1}/V_T$, which has been verified experimentally in a test chip. For the fast channel, the signal goes directly in the fast shaper. It can be noted that the input impedance starts increasing past 10 MHz, then referred to as "inductive behaviour" which can lead to oscillation with a capacitive detector. Integrated technology with careful transistor dimensionning allows to minimize this effect.
With this super common base stage, the input impedance can be decreased from about 2kΩ to 50-80 Ω. Fig. 2.9 shows the simulation of the input impedance without a resistor 50Ω inside the pad.

Two copies of the input current are made available, one for the fast channel to obtain the time information of the particle interaction with the detector, and the other for the slow channel to measure the charge. For the slow channel, the current which goes out from the mirror, is converted into a voltage signal in a RC cell (R=30kΩ and C=10 pF). The global transfer function is given by:

$$V_{out}/I_{in} = -R/(1 + sRC) \text{ with } \tau = RC = 300 \text{ ns}$$

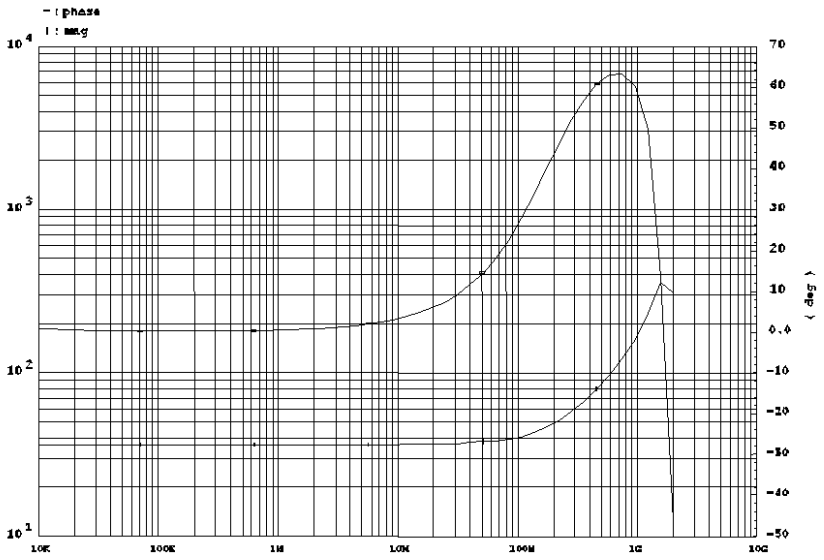

Figure 2.9: *Preamplifier Input impedance (simulation). The top curve shows the phase as function of the frequency (right hand side scale). The bottom curve shows the magnitude (left hand side scale)*

2.2 Charge measurement architecture

2.2.1 Slow Shaper design

To minimize the sensitivity to peaking time variation and time of arrival, the voltage pulse available on the RC integrator is shaped by a $CRRC^2$ shaper with $\tau = 10$ ns. The shaper is included in a Sallen-Key structure, which has been implemented since version-2, and whose schematics is reported in Fig. 2.10. In order to minimize pedestal variation from channel-to-channel slow shaper DC offset dispersion, a differential input stage has been used.
The shaper transfer function is given by:

$$H(s) = \frac{GR_2C_2}{s^2R_1R_2C_1C_2 + \alpha s + 1 + \frac{R_1}{R_3}}$$

With :

$$\alpha = R_1C_1 + [R_1 + R_2 + (1 - G)\frac{R_1R_2}{R_3}]C_2 \text{ and } G = \frac{R_4 + R_5}{R_4}$$

Fig. 2.11 shows the amplifier architecture. To reduce the offset, the amplifier has a bipolar NPN differentiel pair on its input stage. The design of this stage make a centroid as symmetric as possible and a PMOS transistor was added on the non-inverting side.

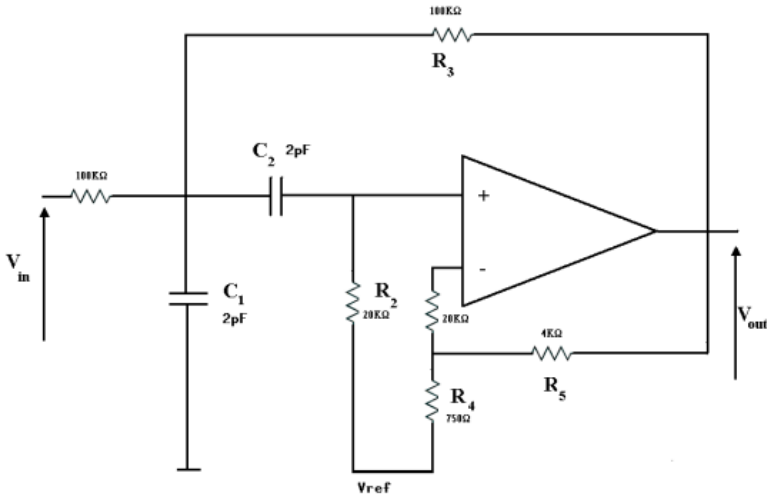

Figure 2.10: *Sallen-key Structure*

The slow shaper open loop transfer function is shown in Fig. A.42 in Appendix A. The amplifier is characterized by a gain band width product GBW =720 MHz, an open loop gain G_0=720 and a dominant pole at $w_0 = 1$ MHz.

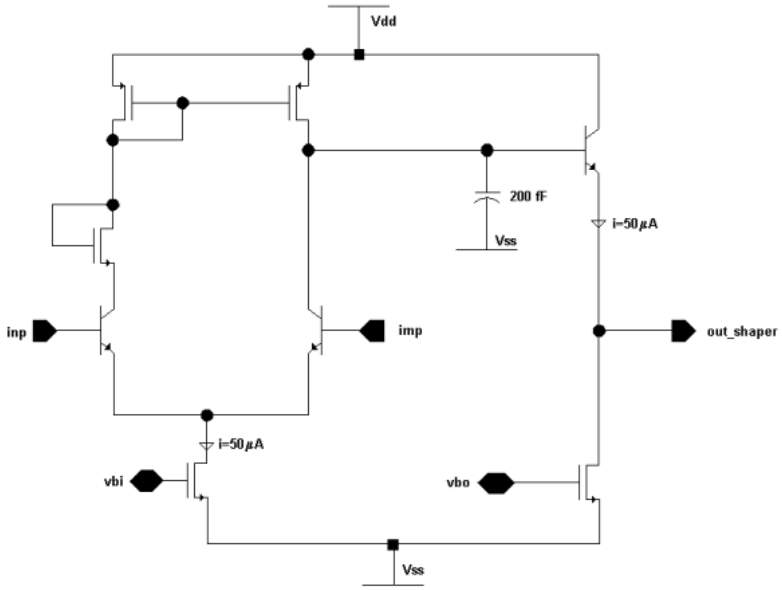

Figure 2.11: *Slow shaper amplifier architecture*

2.2.2 Track & Hold and multiplexing

The preamplifier and the shaper, described in details in the previous sections, are followed by a basic track and hold system and a multiplexed output. Corresponding schematics is displayed in Fig. 2.12. The maximum of the slow shaper output signal is stored in a 2 pF capacitance.

When a trigger signal occurs, all the capacitors are read sequentially through a shift register made by D-flip-flop.

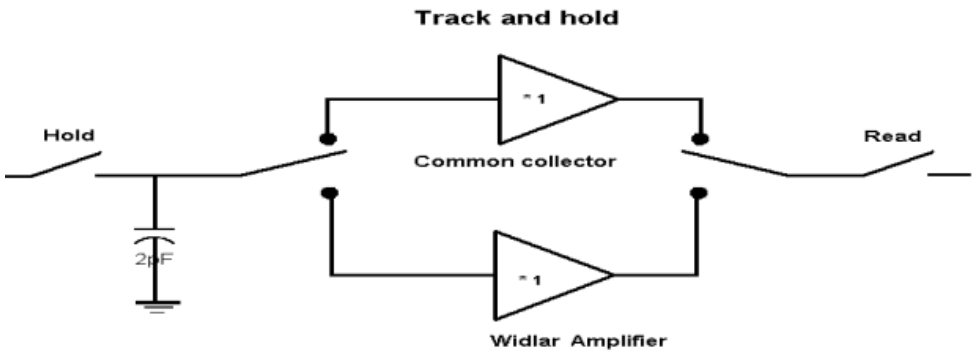

Figure 2.12: *Schematics of the Track and Hold architecture: general view*

In order to fully benefit from such improvement in the charge measurement, the track and hold architecture has been improved compared to the previous versions of the ASIC, as Track & Hold buffer accounts for about 50% of the total DC offset spread. Consequently a new buffer structure with a Widlar differential configuration has been implemented. NMOS transistors have been used to have no leakage current. Fig. 2.13 shows the Widlar configuration of the Track & Hold buffer.

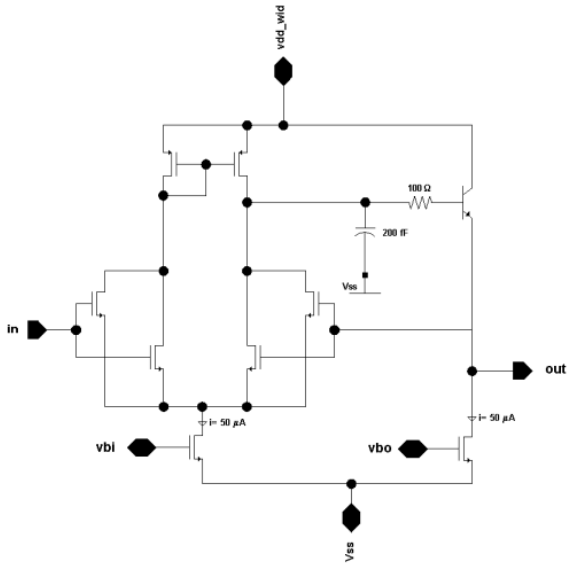

Figure 2.13: *Widlar configuration of the Track and Hold system*

As this configuration had not been tested at the time of the chip submission, the version-2 buffer with a common collector configuration has been kept for every channel. The choice among the two options is ensured by the use of a switch on the input and output common to all channels,

as shown in Fig. 2.12. Simulation of the Track& Hold system is shown in Fig. 2.14 for an input charge of 1 photoelectron.

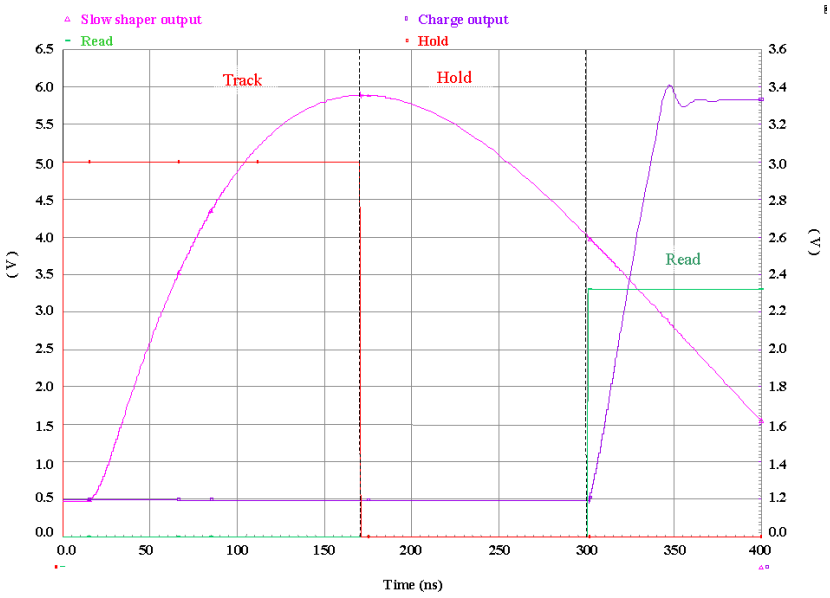

Figure 2.14: *Track and Hold, Read of the signal*

2.3 Trigger architecture

2.3.1 Fast Shaper design

The fast shaper is directly fed with the second mirror output via a 3 pF capacitance and is integrated in a 0.1 pF charge amplifier. The time constant of integration is 10 ns to produce a fast signal and a differential input is used to minimize offset dispersion and allow a common threshold for the chip with a minimal threshold spread. Fig. 2.15 displays the new fast shaper architecture.

The simulated open-loop performance are shown on Fig. A.43 in Appendix A. The open loop gain is G_0=220, the gain bandwidth product GBW=220 MHz, and a dominant pole is found at w_0=1 MHz. The phase margin is about 40^0.

2.3.2 Comparator output

The trigger path is composed of the fast shaper seen in the previous paragraph, followed by a comparator. Schematics of this comparator is given in Fig. 2.16. The input stage of this comparator is designed by a bipolar differential pair in order to minimize the offset. With a low offset comparator and a high gain in the shaping just before, a common threshold can be used for all channels. All the comparators outputs are "ORed" to give a trigger decision for acquisition. A mask register has been added in order to disable a too noisy or defect channel.

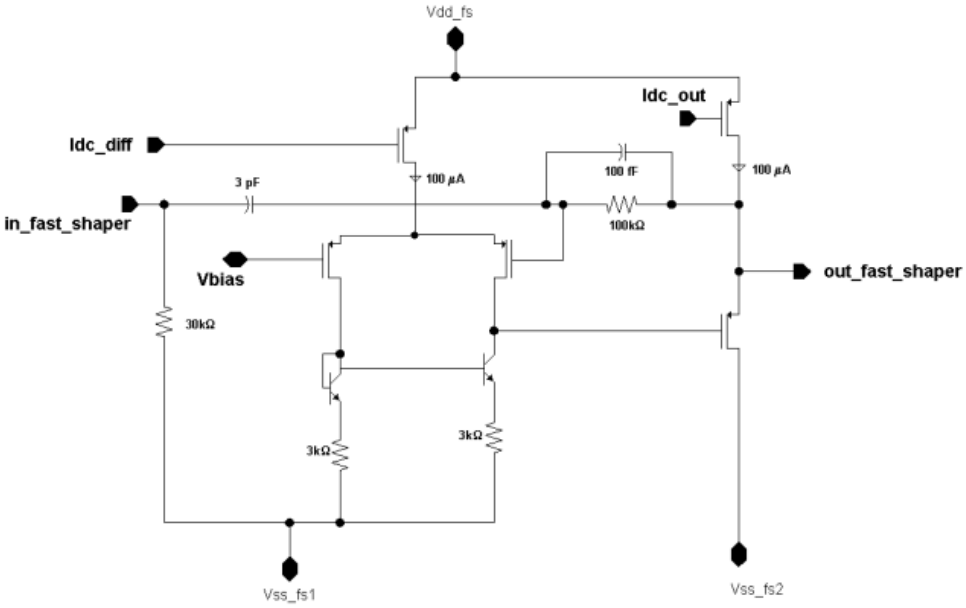

Figure 2.15: *Fast Shaper Architecture*

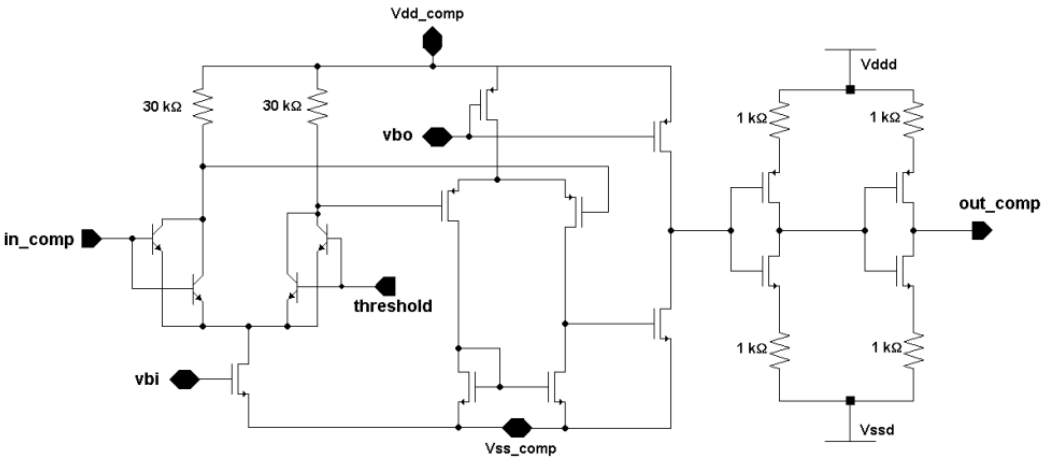

Figure 2.16: *Schematics of the trigger comparator*

Fig. 2.17 displays output from the simulation of the comparator outputs for several values of injected charge.

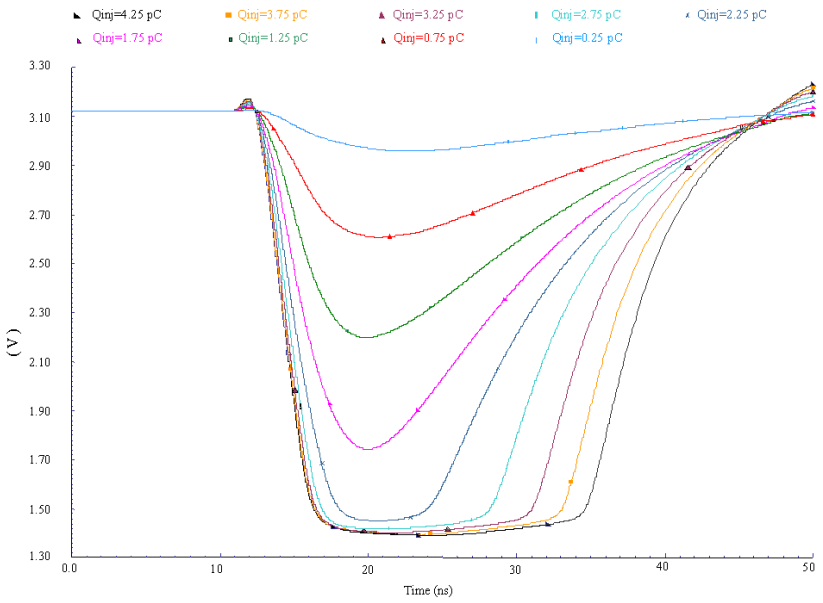

Figure 2.17: *Simulated trigger comparator output for injected charges ranging between 0.25 pC and 4.25 pC, corresponding to 1.5 p.e. and 26 p.e.*

2.4 ASIC simulation

The layout of the ASIC have been designed within the *CADENCE-VIRUTOSO* framework[9]. Simulations of the chip behaviour have been conducted using the *ARTIST* software [10]. Performance have been checked for single channel at different stages of the chip. Fig. 2.18 displays intermediate signals seen at the preamplifier, slow shaper, fast shaper and comparator stages for an input charge of 1 photoelectron and a gain correction set at 1.

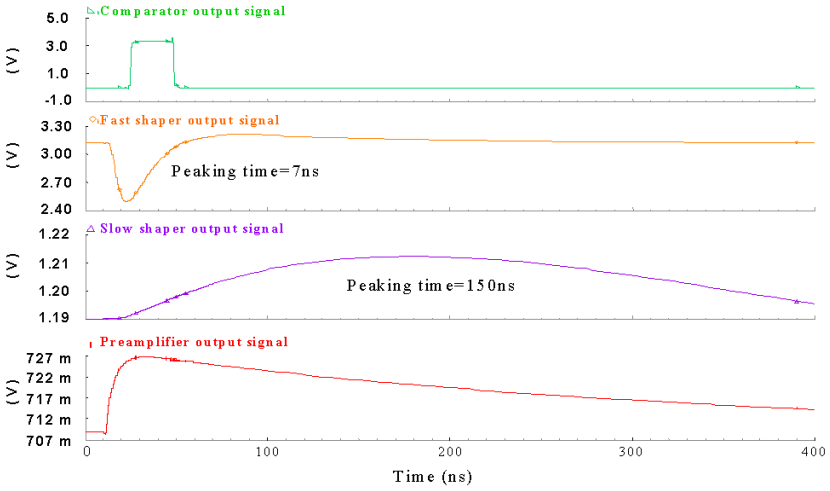

Figure 2.18: *Signals as seen at the preamplifier, slow and fast shaper stages*

3 Performance of the FE electronics ASIC

Performance of the ASIC has been measured using a test card and test equipment designed and constructed by Bern University. Both a Version-1 and a Version-2 of this chip have already been successfully tested. Corresponding results are reported respectively in Ref. [7] and Ref. [8] and constitute the reference to evaluate the performance of this last upgrade. Processus of validation of the present chip is recalled and the results of the systematics studies conducted on the ASIC are detailed in vue of its validation for physics use. Note that, in the following, an input charge of 1 photoelectron corresponds to 160 fC, assuming a photomultiplier gain of 10^6 and a preamplifier gain of 1.

3.1 Variable gain preamplifier

The ASIC preamplifier is a low-noise, variable gain preamplifier device. It is aimed at correcting for non-uniformity seen with the multi-anode photomultiplier tubes H7546, and is also constrained by the need to discriminate single-photoelectron signal from the electronic noise with a good separation.

The preamplifier gain is found to be 60 mV/pC (10 mV/p.e.) with a peaking time of 30 ns for a gain 1.

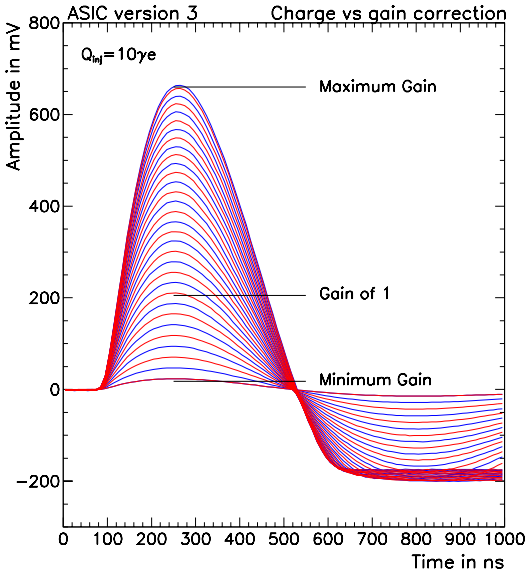

Figure 3.19: *Slow shaper output waveform for a 10 p.e. input charge. 32 out of the possible 64 levels of preamplifier amplification*

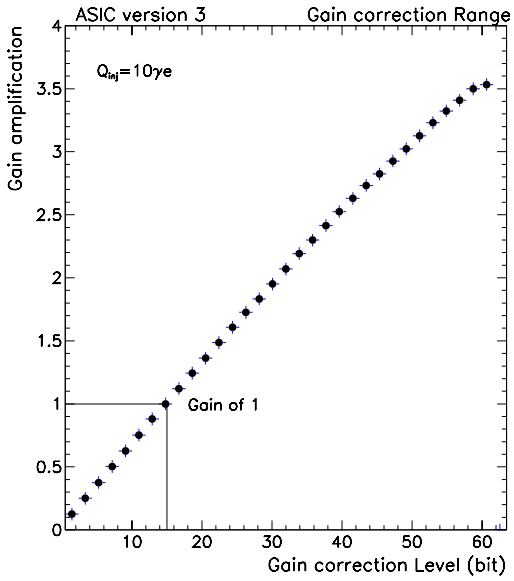

Figure 3.20: *Effective gain amplification as function of the preamplifier level settings*

3.1.1 Gain correction

Six current mirror branches allow to add to the initial signal respectively 2, 1, 1/2, 1/4, 1/8 and 1/16th times the input current. The corresponding 6 switches thus allow to set 64 amplification levels of correction per channel, ranging from 0, where the channel is disabled, to a theoritical value of 63/16 times the input, by steps of 1/16. All levels of gain amplifications have been applied to a fixed input signal. The corresponding output (slow shaper) waveforms are shown in Fig. 3.19 for 32 levels of correction levels. The one-to-one correspondance between the bit correction level and the effective gain is shown in Fig. 3.20. The 64 possible levels are proved to be reliable up to a maximal gain amplification of 3.5. The 6-bit level corrections have also been tested for each bit independentely, with their appropriate weight, and are shown in Fig. 3.21. We conclude that the correction range allowed by the chip satisfies the Target Tracker requirements, asking for a maximal correction amplitude of a factor 3.

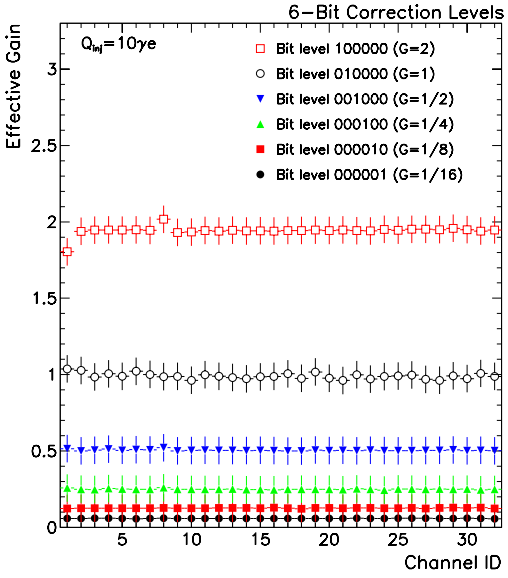

Figure 3.21: *Test of the 6-bit correction levels performed on the 32 channel ASIC. Corresponding gains are 2, 1, 1/2, 1/4, 1/8 and 1/16.*

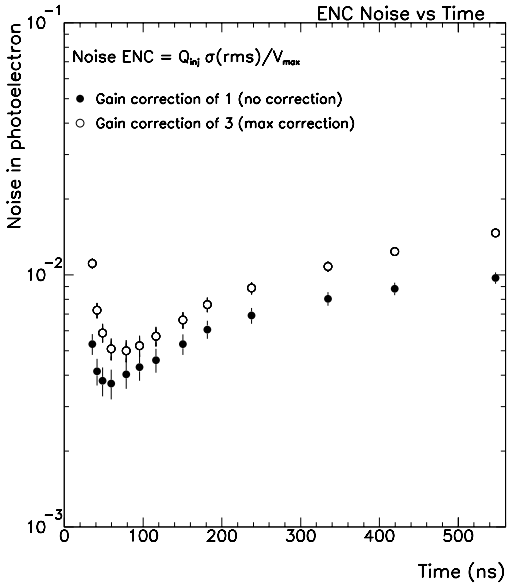

Figure 3.22: *Noise RMS at the preamplifier stage as function of the time constant*

3.1.2 Preamplifier noise

Equivalent noise charge (ENC) at the preamplifier input has been measured as function of shaping time constant, and is displayed in Fig. 3.22. For a timing corresponding to both the fast shaper time constant (10 ns), the noise RMS is found at or below 1% of photoelectron, which does not affect significately the trigger capability.

3.2 Auto-triggering

For all channels, charge is integrated and stored upon a trigger decision in a Track-and-Hold system. A positive trigger decision is taken if at least (any)one of the 32 fast shaper channels detects a signal above a certain threshold. The threshold value is set at once, externally, and is applied to all 32 channels. While emphasis has been put to ensure that trigger efficiency is 100% as low as $1/3^{rd}$ of photoelectron, it is also desirable to avoid large threshold offsets among the 32 channels.

3.2.1 Fast shaper characteristics

Fast shaper is characterized by a gain of 2.5 V/pC ie 400 mV/p.e. for a preamplifier gain set at 1 with a peaking time of 10 ns. The gain becomes 6.0 V/pC for a maximal preamplifier gain settings, which corresponds to 270 mV/p.e. assuming that the gain correction factor of 3.55 is used for correctly compensating the gain spread of the PMTs for the charge measurement. Fig. 3.23 displays the output waveforms from the preamplifier for several input charges.

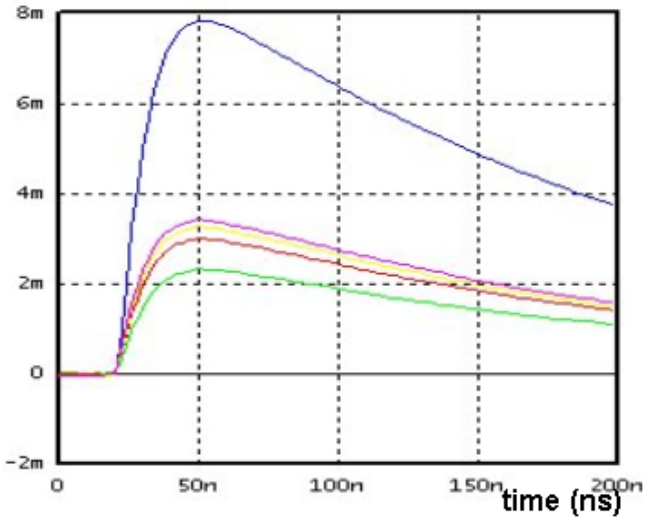

Figure 3.23: *Output waveform measured at the Fast Shaper for a set of gain correction ranging from 1 to 3. Note that fast shaper characteristics are only directly accessible via the test channel 33, readout externally (which results in the observed slew rate). Characteristics are given in the text*

3.2.2 Comparator Output and time walk

Fast shaper ouputs are compared to an adjustable threshold and "ORed" at the comparator stage. In the case where at least one channel is above the threshold, a trigger decision is taken and signal is sent to store signals out of slow shapers 200 ns later.
The output signal from the comparator is a 5 V signal as seen in Fig. 3.24. Fig. 3.24 also shows trigger comparator inputs as function of the time for input charges corresponding to 1/8th, 1/4th, 1/2, 1, 10 and 100 photoelectrons respectively. The trigger rise-time only slightly depends on the input charge magnitude, since a factor 1000 increase in the input signal only results in a 14 ns delay in the trigger desicion. Delay in the trigger time between a given input

charge and an input corresponding to 100 photoelectron is shown in Fig. 3.25 as function of the input charge. Again no difference exceeding 14 ns are seen and we conclude that this delay has no noticeable effects on the chip performance from the physics standpoint.
Time walk does not significantly affect the charge measurement since a 10 ns variation of the sampling time only correspond to a relative change of a few 1/1000 of the charge. Regarding the time measurement, and given the attenuation factor in the 6 meter long scintillators, this delay is not significant either from the physics standpoint since no precise time measurement is needed on the scintillator ends.

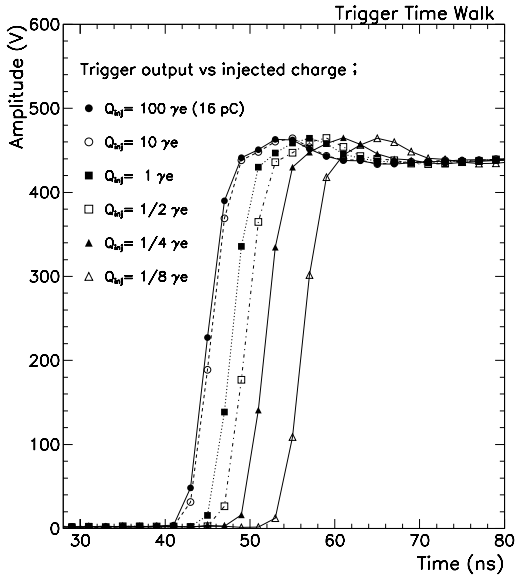

Figure 3.24: *Time walk for the output trigger signal. Trigger response is shown for input charges ranging between 100 p.e. and 1/10 p.e.*

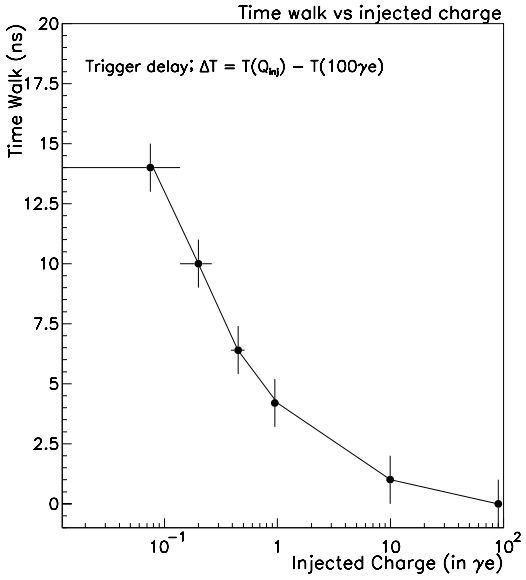

Figure 3.25: *Time walk as function of the injected charge in ns. Delay is computed for each charge and compared to the one corresponding to* $Q_{inj} = 100 p.e.$

3.2.3 Trigger efficiency

Trigger efficiency has been measured as function of the input charge for each individual channeland. Obtained S-curves are displayed in Fig. 3.26 for all 32 channels. It appears that the chip is fully efficient for input charge as low as 1/10th of photoelectron.
Since the trigger threshold is set externally at once for all channel (and can be tunned according to the physics needs), the threshold spread among the 32 channel must be controlled. Fig. 3.27 shows the 50% trigger efficiency thresholds distribution, measured among all 32 channels. Threshold spread is shown to remain around 0.04 photoelectron. This validates the design

based on differential shapers used in this ASIC and represents a significant improvement compared to the previous chip versions, which showed a 0.1 photoelectron spread [8].
Preamplifier gain settings on input are expected to modify trigger thresholds distribution and spread. To assess the amplitude of such effects, measurements have been repeated for two different gains. As preamplifier gain amplification is set from 1 to 3, the S-curves are moved towards lower values, as seen in Fig. 3.26 (as expected since from the same input charge amplified by higher factor) with a 50% trigger efficiency threshold decreased by a factor of about 2.5 in average, see Fig. 3.27. The slight difference with the expected factor 3 is due to a small change in risetime between gain 1 and a gain 3 signals, as described in the last Section 3.2.2. For the same settings, trigger threshold spread is also reduced, as expected.

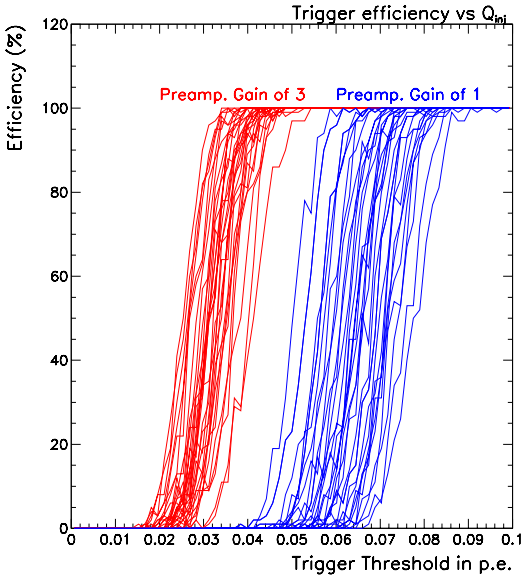

Figure 3.26: *Trigger efficiency (S-curve) as function of the input charge for the 32 channels for a preamplifier gains of 1 and 3*

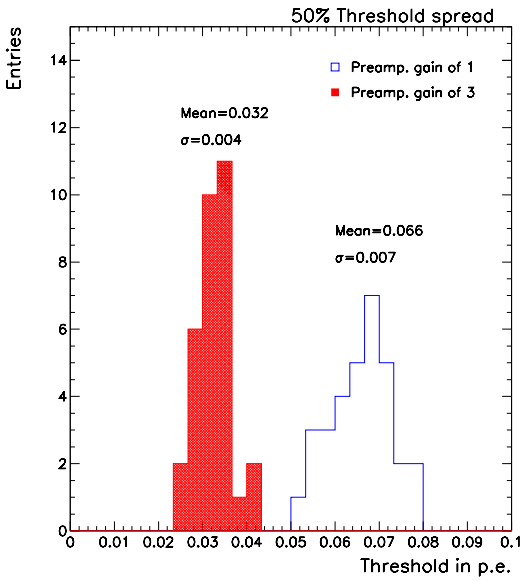

Figure 3.27: *50% trigger efficiency threshold dispread for all 32 channels for a preamplifier gains of 1 and 3*

3.2.4 Fast shaper Noise

Noise at the fast shaper input has been determined in Section 3.1.2. Noise at the fast shaper output has been assessed by two ways: it can be measured directly using the intermediate outputs of a test channel located on the same chip (channel 33) or it can be indirectly extracted from the S-curves using the slope at the 50% trigger efficiency point.
Direct measurement provide results of about 1.5 mV found for a fast-shaper amplification factor of 800 mV/p.e. at a gain 1, and 3.3 mV for a gain of 3, well below 1% of photoelectron. An average value of about 1.5 mV is found for a gain 1, which is consistent with direct results.

These results show that the noise level dos not exceed a few 1/1000 of photoelectron, which are to be compared with a trigger threshold value of 1/3rd of photoelectron used for physics purposes. We conclude that electronic noise should not be a problem in the working conditions of the OPERA Target Tracker as far as trigger capabilities are concerned. Another important issue is the spurous trigger rate. Measurements have been performed for a long period of time and no charge injected in the chip. Trigger rates are determined to be well below 10^{-3} Hz (no trigger signal in 1 hour) for a threshold of 0.1 p.e.

3.2.5 Hit Register

Although not required in the baseline, a hit register has been implemented in the new ASIC. It produces the sequential list of all channel trigger status. This functionality has been tested and found to work well. However, significant cross-talk with neighbouring channels is seen in the register output, as soon as the injected charge is about 100 times the trigger threshold value. Thus, for a typical 0.2 p.e. threshold, any channel above 20 p.e. will induce cross-talk in the neighbouring channels, that will make those ones to be declared with a trigger ON. It has to be noticed that this affects only the hit register output. This problem is not considered as important since the information provided by the hit register is already a redudance of the multiplexed charge measurement.

3.2.6 Summary

Table 2 reports the characteristics and performance of the auto-trigger functionalities used in the ASIC version 3, and shows a comparison with the results obtained with version-2.

	ASIC version 2	ASIC version 3
- Fast shaper peak time	20 ns	10 ns
- Fast shaper gain (Gain 1)	1,3V/pC (208 mV/p.e.)	2.5V/pC (400 mV/p.e.)
(maximal Gain)	3.6V/pC (202 mV/p.e.)	6.0V/pC (270 mV/p.e.)
- Threshold spread	0.1 p.e	0.03 p.e.
- Fast shaper noise (Gain 1)	2.0mV (1.5fC or 0.01p.e.)	1.8mV (0.72fC or 0.005p.e)
(maximal Gain)	4.0mV (1.1fC or 0.02p.e.)	3.3mV (0.55fC or 0.012p.e)
- Trigger sensitivity	100% at 0.3 p.e.	100% at 0.1 p.e.
- Hit Register	None	Implemented

Table 2: *Auto-trigger characteristics and performance*

3.3 Charge measurement

The input signal can be pre-amplified independently for each individual channel of the ASIC. This latter is then transmitted to both fast and slow shapers for trigger and charge measurement respectively. The important charge measurements characteristics are the slow shaper gain and peaking time, the channel-to-channel offset. The "figure of merit" of the charge measurement is the linearity of the response. All these points are featured in the next subsections.

3.3.1 Slow shaper characteristics

Fig.3.28 displays the waveform output of a single channel for input charges ranging from 1 to 100 photoelectrons with a preamplifier gain set to 1. The full response range is set from a few mV corresponding to a fraction of photoelectron to 2.0 Volts for a 100 p.e. input charge. Main characteristics are the gain and the peaking time.

Slow shaper gain

Slow shaper maximum amplitude values V_{max} have been measured for all 32 channels of the chip for an input charge of 10 p.e., and are reported in Fig. 3.29 as function of the channel ID. For a preamplifier gain set to 1, these values correspond to an average gain of 19.4 ± 0.2 mV/p.e., which is equivalent to about 121 ± 1 mV/pC. Results are quite stable among channels since channel-to-channel variations show an RMS of 0.08% (gain 1) and 1.5% (gain 2.75), as seen in Fig. 3.30.

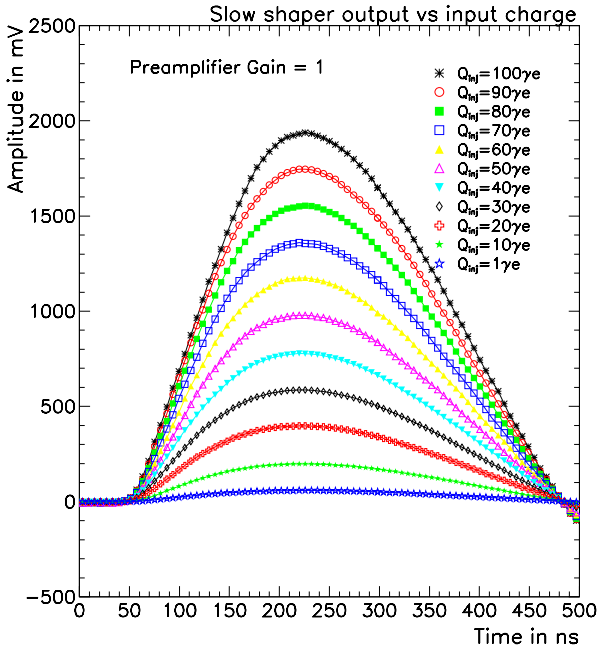

Figure 3.28: *Slow shaper waveform outputs for different input charge corresponding to 1, 10, 20, 30, 40, 50, 60, 70, 80, 90 and 100 photoelectrons*

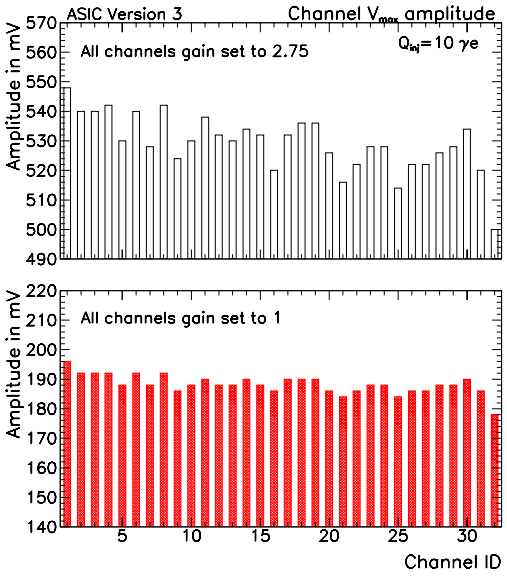

Figure 3.29: *Gain as function the channel ID for both a gain 1 and am effective gain correction of 2.75 (top plot) for an input charge of 10 p.e.*

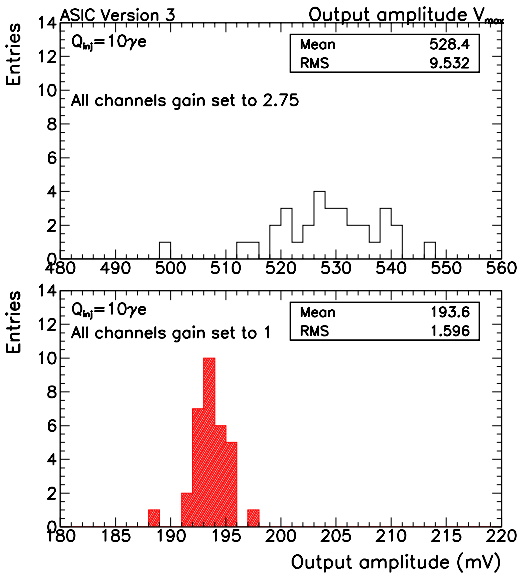

Figure 3.30: *Maximum amplitude V_{max} distribution for an input charge of 10 p.e. at a gain 1 (bottom) and a gain 2.75 (top)*

Slow shaper peaking time

The peaking time has been determined for all 32 channels and reported in Fig. 3.31 for an input charge of 10 p.e. and a gain 1, as function of the channel ID. An average value of about 159 ± 1.7 ns is derived with a distribution spread below ± 4 ns, as seen in Fig. 3.32.

Peaking time is shown to depend slightely upon the input charge, since it decreases by about 6 ns as the input charge is increased from 1 to 100 p.e., as shown in Fig. 3.33 for a single channel. Consequentely, we expect a slight dependence upon the preamplifier gain, as one goes from a gain 1 to a gain 2.75. The average peaking time is indeed decreased from 162 ns to 159 ns as all channels preamplifier gains are set to 2.75, see Fig. 3.32. Peaking time spread is shown to be unsensitive to the gain, with a 6 ns dispersion in both cases. For input charges above 120 photoelectron, where saturation effects become significant, the shift does not exceed 10 ns in total, as shown in Fig. 3.33.

The choice of longer time constant for the slow shaper, as compared to the previous version of the ASIC, is justified by the need to avoid any significant variation on the charge measurement as the sampling time is varied by ± 10 ns. This choice allows the user to be rather independent of the input charge magnitude as well as of the trigger time.

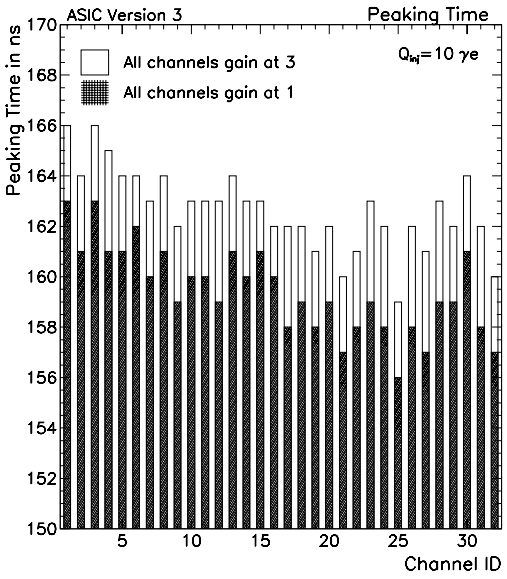

Figure 3.31: *Peaking Time for an input charge of 10 p.e. as function of channel ID as all channels are set to a gain 1 (lines) and to a gain 3 (plain)*

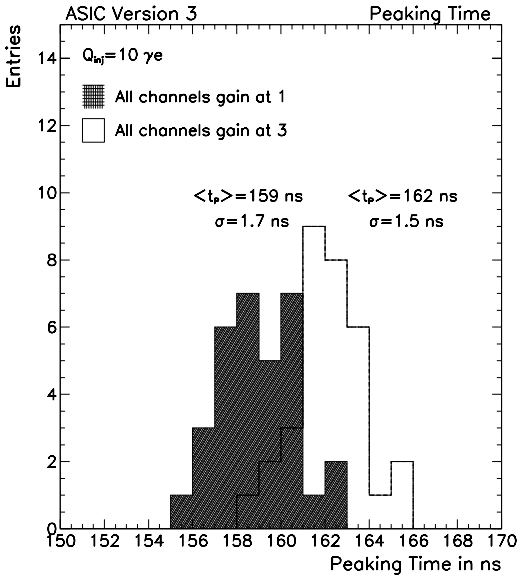

Figure 3.32: *Peaking Time distributions for a 10 photoelectron input charge when all channels are set to a gain 1 (lines) or to a gain of 3 (plain)*

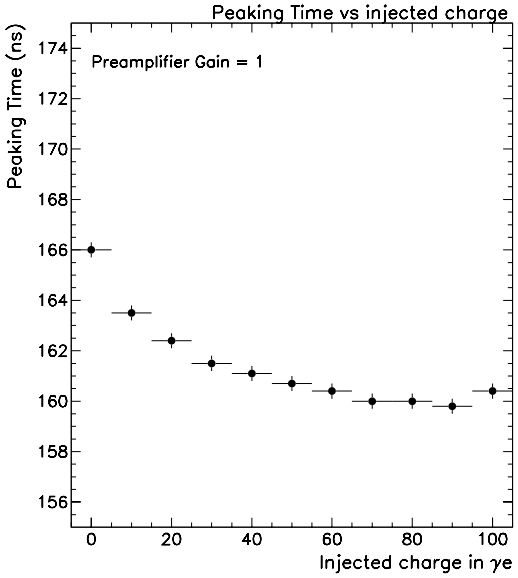

Figure 3.33: *Peaking Time as function of the injected charge for a single channel (channel 08) with a preamplfier gain of 1. First point is obtained for an injected charge of 1 p.e. Channel to channel variation are extracted from the previous plot.*

3.3.2 Channel-to-channel offset (pedestal)

Upon a trigger decision, slow shaper signals are captured by a Track& Hold system. This Track & Hold has been designed to offer two distinct structures to store the maximum voltage amplitude: a classical common collector (CC), and a Widlar option, as defined in Section 2.3. The user can choose via a simple hardware switch between the two options. Measured pedestals are thus given for both structures.

Pedestals are given by V_{DC} voltage levels. They have been measured for all individual channels and V_{DC} values reported as function of the channel number in Fig. 3.34 for both CC and Widlar options. V_{DC} average is about 2190.0 ± 3.3 mV for the CC measurement and about 1205.0 ± 2.6 mV for the Widlar. Corresponding maximum spread is ± 8 mV in the first case (CC) while it is about ± 6 mV with the Widlar, as seen in Fig. 3.35. These values correspond to less than a 1/3 of photoelectron pedestal spread in the charge determination.

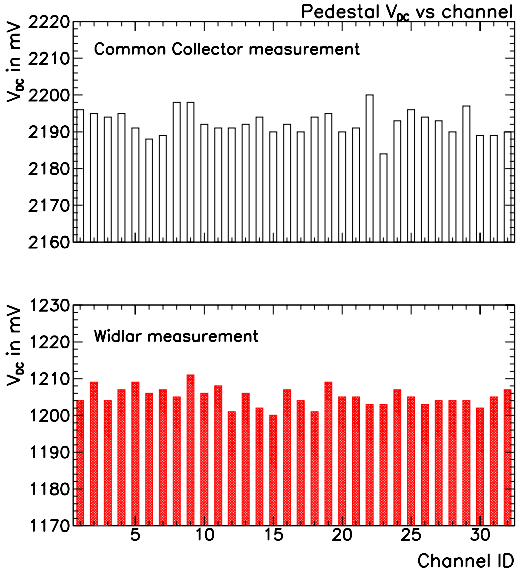

Figure 3.34: V_{DC} *measured for 32 channel with the common collector (CC) (top) and with the Widlar (bottom plot)*

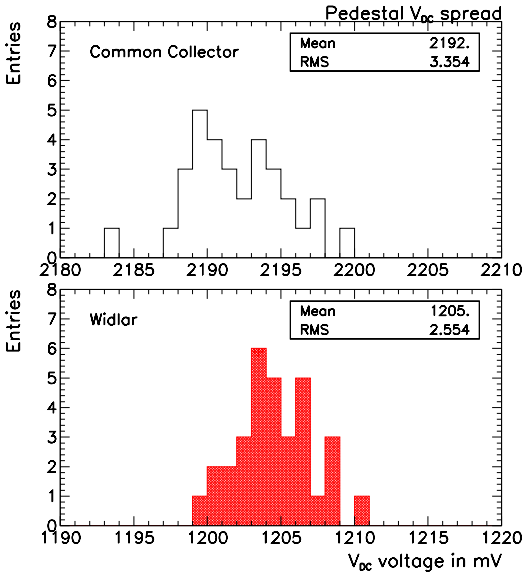

Figure 3.35: V_{DC} *distribution measured with the Common collector (CC) (top) and with the Widlar (bottom plot)*

These results constitute significant improvement with respect to pedestals seen in the previous chip version, which were measured at ± 18 mV for an equivalent gain. This is explained by the choice of a Sallen-Key structure for the slow shaper, and by the differential shapers in the Widlar structure used to store the charge. The remaing spread comes from two identified sources, about 50% from the slow shaper, and 50% from the Track & Hold buffer and may be taken care of by appropriate offline corrections.

3.3.3 Linearity of the charge measurement

The linearity in the charge measurement has been assessed for all channels as function of an input charge ranging between 1 and 100 p.e. It has been controlled for different value of gain corrections.

Linearity for a gain 1

Fig. 3.36 displays the readout charge for channels 1, 8, 16, 24 and 32 as function the charge injected, and compares it with the results of a linear fit, while Fig. 3.37 shows the residuals computed as the difference between measurement and the fit. No deviation above 2% is seen over the full [1-100] photoelectrons range. This result constitute an improvement compared to previous chip version measurements, where the linearity was better than 1% over a smaller range from 0 to 75 photoelectrons.

We note that the fit results depend upon the weight affecting every data points, which can be tunned so that to improve the linearity of the measurement in a specific area. We also note that, as already mentionned with version-2, the dynamic range can be further extended by increasing the supply voltage (V_{dd}) from the present setting of 5 V. Indeed the choice of the AMS BiCmos technology makes it possible to set this value up to 7 V with no expected performance deterioration.

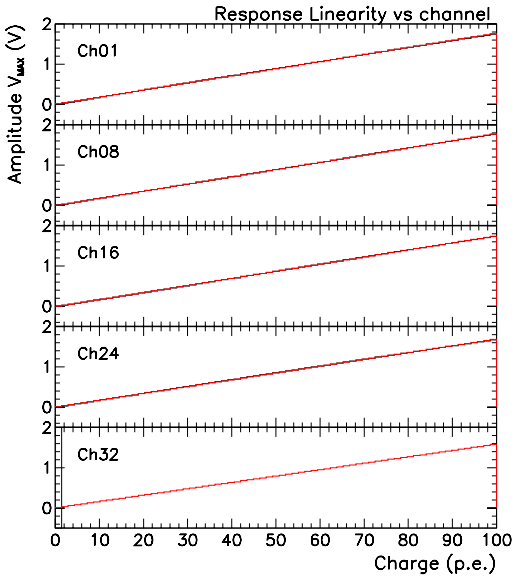

Figure 3.36: *Response linearity in the charge measurement as function of the input injected charge for channel 01, 08, 16, 24 and 32*

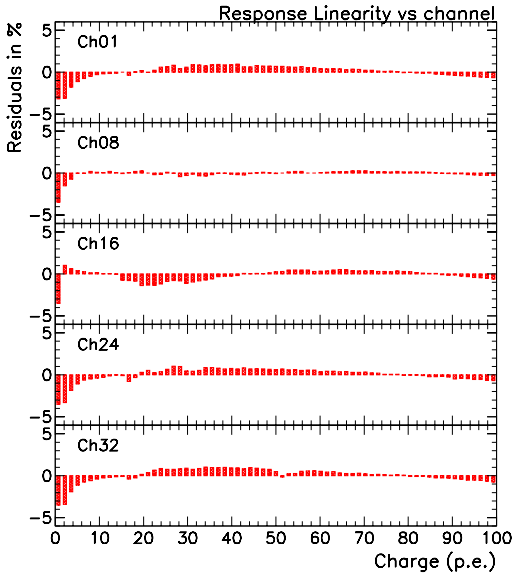

Figure 3.37: *Response linearity residuals as function of the injected charge for channels 01, 08, 16, 24 and 32*

Linearity at higher gain

The dynamic range depends upon the preamplifier gain settings. Fig. 3.38 shows the effects of increasing the gain setting of a single channel from a gain of 1/2 to a maximal effective gain of 3.55. A very good linearity is found up to at least 16 pC, ie: 100 p.e. at gain 1. No significant effect is seen up to effective gains of 2.0 and 3.55 respectively, with corresponding upper values of 12 pC, ie: 150 p.e. at gain 2, and 4-5 pC ie: 90-110 p.e. at gain 3.55. This result represents a significant improvement with respect to version-2 ASIC, as reported in Ref. [8]. We conclude that the present ASIC provides a large dynamic range, even in the worse case scenario where an amplification by a factor 4 is needed to an indivudual channel.

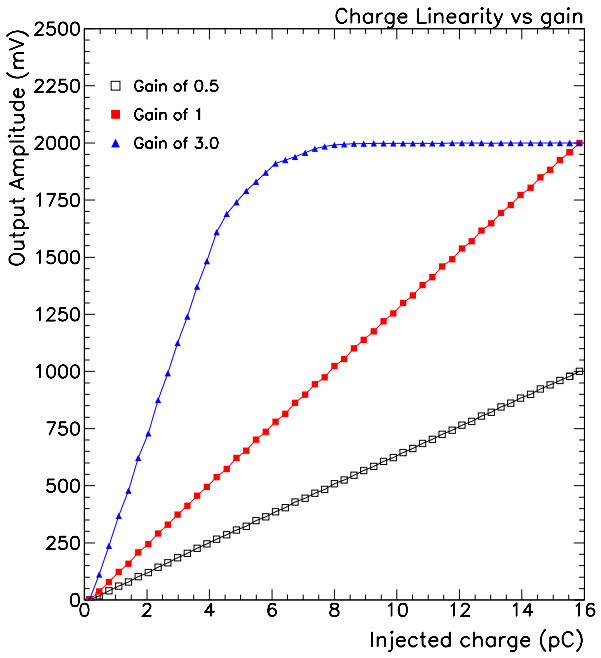

Figure 3.38: *Linearity of the charge measurement as function of the input charge for a gain set at 0.5, 1, 2 and a maximum value of 4.0 (3.5 effective). Note that a photoelectron corresponds to 160 fC at gain 1, 80 fC at gain 2, and 45 fC at maximal gain of 3.55*

3.3.4 Cross-talk

Cross-talk can affect the physics input to the ASIC. Indeed, such effects are known to be non-negligible for the multi-anode PMTs used for the OPERA Target Tracker. Measurements reported in Ref. [6] for the LHCb experiment show that the magnitude of this "physics" cross-talk between 2 adjacent channels may be as high as 2-3%. This sets a reference value with which we have to compare electronic sources of cross-talks induced in the ASIC itself.

Two kinds of cross-talks are known to affect the charge measurement of any individual channel and have been measured in the previous ASIC versions, reported in Ref. [7] and Ref. [8]. The first cross-talk source is due to a coupling between the trigger and the charge measurement branch, which causes a slight distortion of the charge signal upon a trigger decision. The second source

of cross-talk is seen between neighbouring channels, where a large charge in a single channel can induce a signal in a locally close track. The magnitude of such effects have been assessed with the new ASIC.

Trigger-Charge crosstalk

Trigger-charge couplings can cause the distorsion of the signal waveform. This effect is illustrated in Fig. 3.39, which shows the signal output waveform used to measure the charge, and compares it to the very same waveform obtained upon a trigger decision. It appears that the digital signal (0-2V logic) output from the comparator produces a glitch that can be seen on the corresponding channel. However while this effect is sizeable around the time at which trigger decision occurs, its magnitude at the sampling time is much smaller.

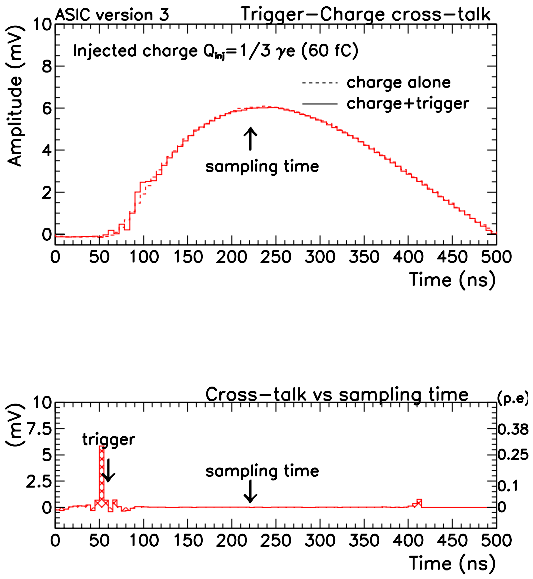

Figure 3.39: *Effects seen on a charge channel due to the trigger-charge couplings. Top figure represents the charge output waveforms with no trigger decision (dashed line) and with a trigger decision. Bottom plot displays the difference of the two waveforms as function of the time. Sampling time is 160 ns after the trigger time.*

In the two previous ASIC versions, the cross-talk magnitude at the sampling time has been shown to be positive and to remain below 0.5 mV [8]. It is now of negative sign and reduced to levels below 0.2 mV, thanks to a reduced trigger output magnitude. This value corresponds to less than 1% photoelectron effect.

This additionnal peak up signal is seen as a coupling between the comparator output and somewhere after the preamplifier, since this phenomenon is independant of the weights applied to the channel. One notices also some influence due to the mask of the channel which receives the input signal. The exact origin of the coupling is probably due to power supply glitch to the comparator. We conclude that trigger-charge cross-talk does not affect significantely the charge measurement.

Channel-to-channel crosstalk

Couplings between neighboring channels may also cause a signal in the hit channel to be seen in the neighbouring channels. Fig. 3.40 displays the output signal for a single channel with an injected charge of 10 photoelectrons, and compares it with the charge outputs observed in the 1st, 2nd and 3rd neighbouring channels. It is shown that the charge induced by cross-talk has a negative sign and a magnitude well below 0.2-0.5 mV which correspond to 0.1-0.25% of the input charge at the sampling time. The effect is maximal in the 1st neighbour, as expected, but never completely vanishes, whatever the channel location may be.

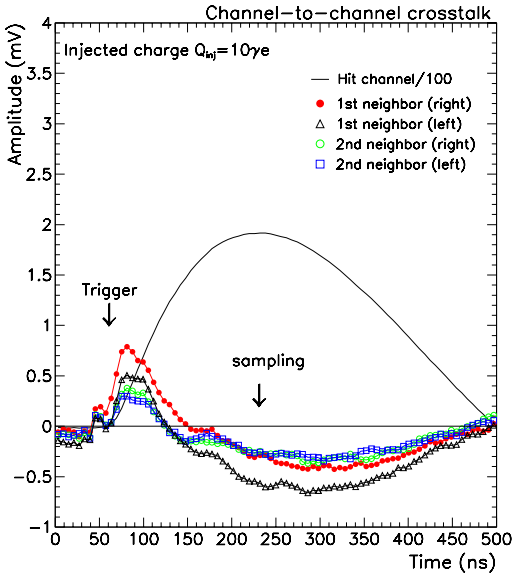

Figure 3.40: *Signal output for a channel with an injected charge of 10 p.e. divided by 100 and charge induced in the 1st and 2nd neighbouring channels by cross-talk*

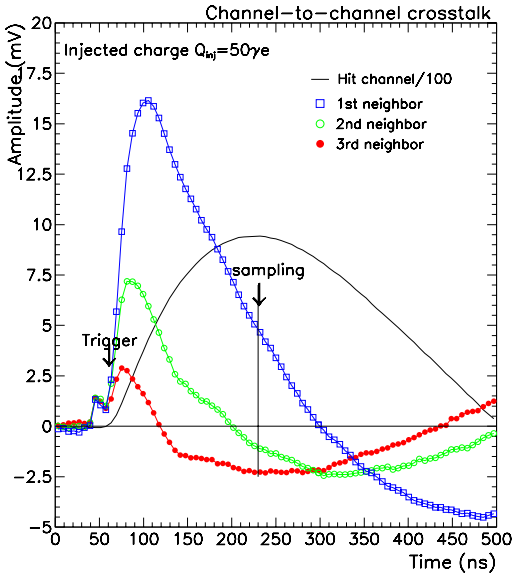

Figure 3.41: *Signal output for a channel with an injected charge of 50 p.e. divided by 100 and charge induced in the 1st and 2nd neighbouring channels by cross-talk*

This seems to show that there are two competing terms in the cross-talk contribution: a first term, of positive sign and mostly significant in the 1st neighbouring channels of the one with the injected charge; and a constant term of negative sign and present in all channels, which is about 0.2% to 0.7% of the input charge depending on the chip.

Cross-talk effects have been assessed for higher input charges, as seen in Fig. 3.41 for a 50 photo-electron input charge. Cross-talk seen in the 1st neighbours is slightly increased, with a positive sign and a magnitude of 0.5% of the input charge. Cross-talks in 2nd and 3rd neighbors (and channels far away) remain constant.

This level of cross-talk in the first neighbouring channel has been further investigated. It is found that by increasing the rise-time of the input signal to the chip, one makes the cross-talk

completely disappear to level below 0.1% of the injected charge. A possible explanation for this phenomenon is the saturation of the preamplifier for sharp input signal. For a 7 ns rise-time signal, which corresponds to typical physics signal out of the PMT, the cross-talk is found negligible at the level of 0.1%. For the full dynamic range, we conclude that cross-talk remains below 1.0% even for charges of 100 photoelectrons.
The cross-talk in non-neighbouring channels can be significantely reduced as we use the multiplexed output to which we subtract channel 0 baseline. This technic is planned for the normal functioning of the OPERA TT read out chip to reduce the dependence to effects common to all channel like (temperature variation etc..). Such measurements show a reduced cross-talk level of about 0.2%.

3.3.5 Multiplexed output

Test results performed at Bern and LAL show no problem in the multiplexing. The output level is around 3V for the maximum amplitude. Trigger mask is now redundant since any individual channel may be completely switched off using the 6-bits register. This will allow to avoid triggering on noisy channel. The readout is clocked at 5MHz and it takes 6.4μs to read the 32 channels (in serie).

3.3.6 Summary

Table 3 reports the characteristics and performance of the charge measurement performed on the ASIC version 3 and shows a comparison with version-2 results.

	ASIC version 2	ASIC version 3
- Dynamic range (Gain 1)	12 pC (75 p.e)	18 pC (110 p.e)
(maximal Gain)	2.8 pC (50 p.e)	4.5 pC (100 p.e)
- Slow shaper peak time (Gain 1)	106 ns	160 ns
(maximal Gain)	115 ns	175 ns
- Slow shaper Gain (Gain 1)	140 mV/pC (22 mV/pe)	125 mV/pC (20 mV/pe)
- Pedestal Spread (mV)	$\pm$18 mV ($\pm$0.8 p.e)	$\pm$6 mV (widlar) / $\pm$9 mV (CC) ($\pm 0.4 - 0.5$ p.e.)
- Noise @ MUX rms (Gain 1)	0.5 mV (4.1fC or 0.026p.e)	1.3 mV (12fC or 0.075p.e)
(maximal gain)	0.85 mV (2,4fC or 0.043p.e)	1.4 mV (3.7fC or 0.08p.e)
- Cross-talk	$\mathcal{O}(0.5\%)$	$\mathcal{O}(1\%)$
Linear Voltage range @ MUX	about 1.8 V to 3.5 V	about 2.2 V to 4.2 V
Clock frequency	5 MHz (6.4μs/32ch.)	5 MHz (6.4μs/32ch.)

Table 3: *Performance of the ASIC version-3 and comparison with the previous version*

4 Conclusion

4.1 Summary of the ROC performance

Table 4 reports the performance as measured on the 32 channel chip. The Version 3 chip performance satisfies all Target Tracker requirements. A 100% trigger efficiency is ensured down to 1/3rd photoelectron, the linearity in the charge measurement is ensured in the [1-100] photoelectron range, and the gain correction at the preamplifier stage has been proved fully functionnal up to a factor 3.5. The present ASIC consitutes an improved version with respect to several aspects of the chips design as reported in Ref. [7] and Ref. [8].

	ASIC version 2	ASIC version 3
PREAMPLIFIER		
- Gain correction	Range 1-2.875 (4 bit)	Range 0-3.5 (6 bit resolution)
	1+(1,1/2,1/4,1/8)	2,1,1/2,1/4,1/8,1/16
- Input for Test Pulse	None	3 pF alternate (even/odd ch)
- Input Impedance	$Z_{in} \approx 2k\Omega$	$Z_{in} \approx 125\Omega$
AUTO-TRIGGER:		
- Fast shaper peak time	20 ns	10 ns
- Fast shaper gain (Gain 1)	1,3V/pC (208 mV/p.e.)	2.5V/pC (400 mV/p.e.)
(maximal Gain)	3.6V/pC (202 mV/p.e.)	6.0V/pC (270 mV/p.e.)
- Threshold spread	0.1 p.e	0.03 p.e.
- Fast shaper noise (Gain 1)	2.0mV (1.5fC or 0.01p.e.)	1.8mV (0.72fC or 0.005p.e)
(maximal Gain)	4.0mV (1.1fC or 0.02p.e.)	3.3mV (0.55fC or 0.012p.e)
- Trigger sensitivity	100% at 0.3 p.e.	100% at 0.1 p.e.
- Hit Register	None	Implemented
CHARGE MEASUREMENT:		
- Dynamic range (Gain 1)	12 pC (75 p.e)	18 pC (110 p.e)
(maximal Gain)	2.8 pC (50 p.e)	4.5 pC (100 p.e)
- Slow shaper peak time (Gain 1)	106 ns	160 ns
(maximal Gain)	115 ns	175 ns
- Slow shaper Gain (Gain 1)	140 mV/pC (22 mV/pe)	125 mV/pC (20 mV/pe)
- Pedestal Spread (mV)	$\pm$18 mV ($\pm$0.8 p.e)	$\pm$6 mV (widlar) / $\pm$9 mV (CC)
		($\pm 0.4 - 0.5$ p.e.)
- Noise @ MUX rms (Gain 1)	0.5 mV (4.1fC or 0.026p.e)	1.3 mV (12fC or 0.075p.e)
(maximal gain)	0.85 mV (2,4fC or 0.043p.e)	1.4 mV (3.7fC or 0.08p.e)
- Cross-talk	$\mathcal{O}(0.5\%)$	$\mathcal{O}(1\%)$
Linear Voltage range @ MUX	about 1.8 V to 3.5 V	about 2.2 V to 4.2 V
Clock frequency	5 MHz (6.4μs/32ch.)	5 MHz (6.4μs/32ch.)

Table 4: *Performance of the ASIC version-3 and comparison with the previous version*

4.2 Proposal

The FE electronic ASIC designed and tested by both LAL and Bern Group is found to satisfy the Target Tracker requirements: the preamplifier stage is proven to be functional and allow to correct for input non-uniformity up to a factor 3.5 with a good precision; the auto-trigger functionality has been tested and found to be 100% efficient at a 1/3rd of photoelectron with a negligible electronic noise; the charge measurement feature has been proven reliable over [0-125] photoelectron dynamic range with a good linearity response (1%) up to 100 p.e. The proposal is that this version should be considered as the baseline version for the OPERA Target Tracker.

References

[1] OPERA Proposal, CERN/SPSC 2000-028, SPSC/P318, LNGS P25/2000 and "Status Report on the OPERA experiment", CERN/SPSC 2001-025, SPSC/M668, LNGS-EXP 30/2001

[2] M.Dracos et al., "Plastic sintillator target tracker proposal and studies done at Strasbourg", OPERA-NOTE 26, 16 June 2001.

[3] CERN Finance Comittee, 290th meeting, 19 June 2002 CERN/FC/4583

[4] R. Arnold, E. Baussan et al, IReS, "Results about H7546 Multianode PMT's studies", OPERA Internal Note #30,

[5] Technology AutriaMicroSystems (AMS) BiCMOS 0.8 microns, see web site for documentation: "http://www.europractice.imec.be/europractice/on-line-docs/prototyping/ti/ti_byq.html"

[6] S. Monteil, and private communication.

[7] "Performance of a FE electronics ASIC for the OPERA Target Tracker: Version-1", Opera Internal note #34

[8] "Performance and Design of a Front End electronic ASIC for the OPERA Target Tracker: Version-2", Opera Internal note #40

[9] *Cadence* software, Design for manufacturing technology, see web site: "http://www/cadence.com"

[10] Software *Artist*

[11] C. de La Taille, G. Martin-Chassard, L. Raux, LAL Orsay, presentations at OPERA Target Tracker meetings, CERN Jul-2001, CERN October 10-2001, CERN Fevrier-2002 accessible on http://www.lal.in2p3.fr/recherche/opera/internal_hard.html

A Slow and fast shaper open loop transfer function

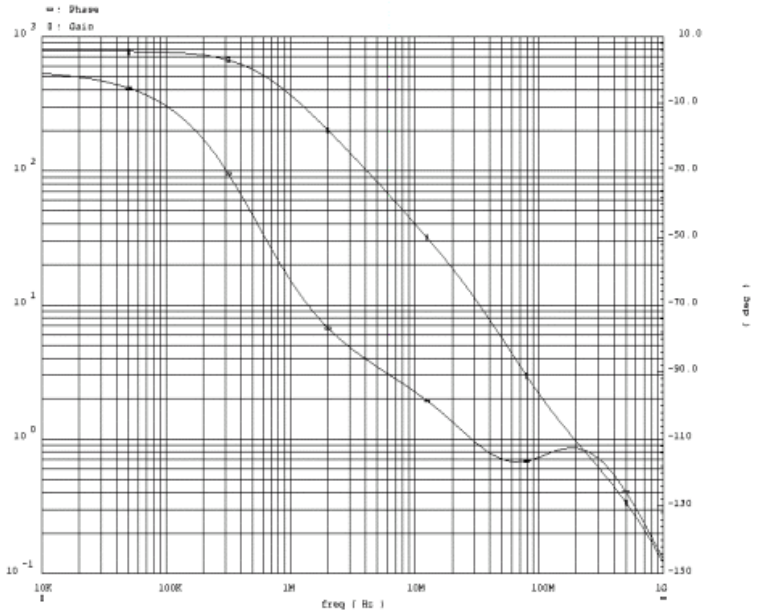

Figure A.42: *Slow shaper open loop transfer function. Top curve shows the phase variation with frequency (right hand side scale). Bottom curve shows the magnitude (left hand side scale)*

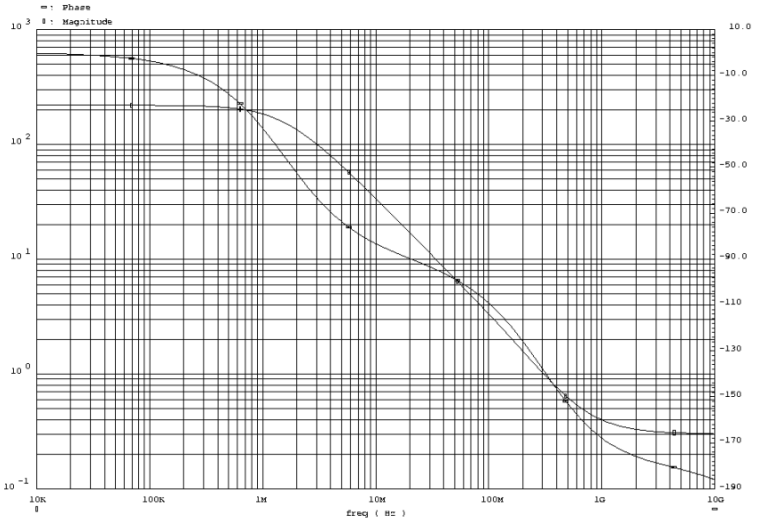

Figure A.43: *Open loop transfer function of the fast shaper amplifier. Top curve shows the phase variation with frequency (right hand side scale). Bottom curve shows the magnitude (left hand side scale)*

B Pinout of the 32 channel ROC

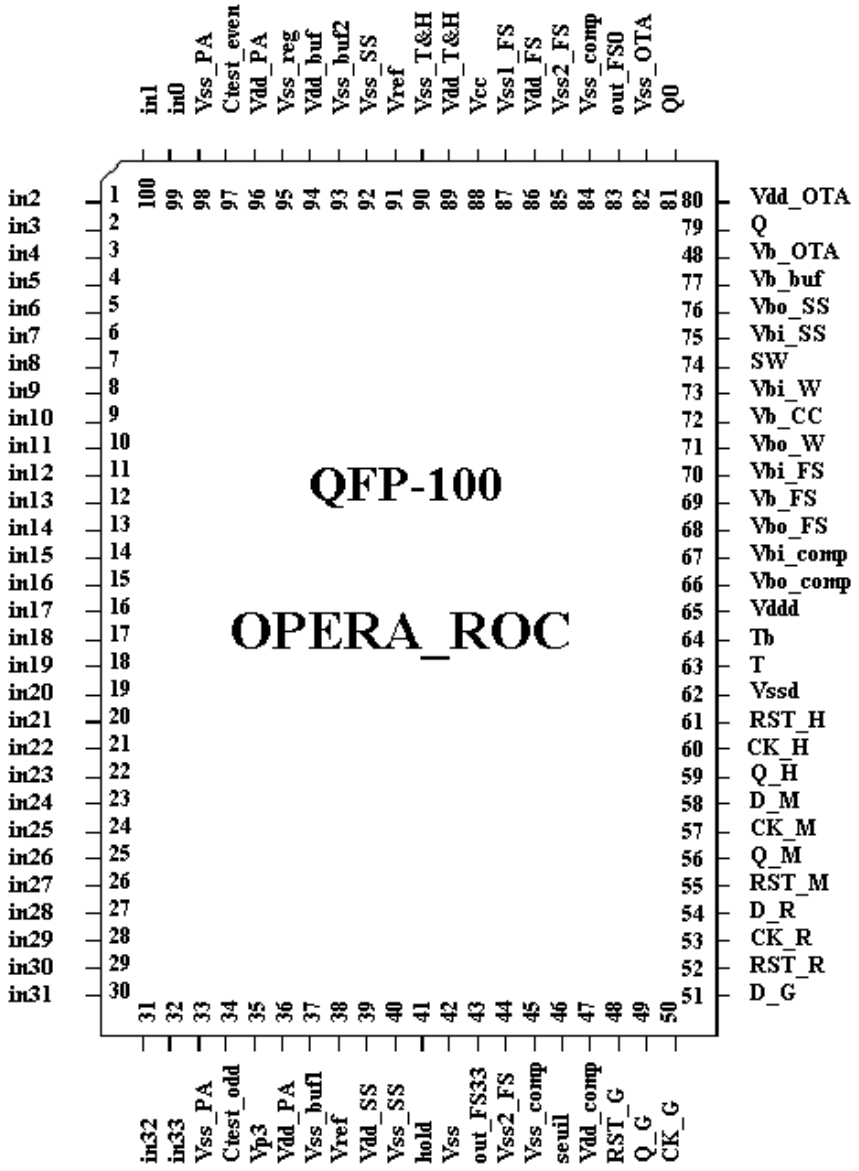

Figure B.44: *Pinout of the 32 channel ASIC*

pin	Name	Description	Comment	Current	DC level
1-31	in2 – 32	input channel 2 to 32			0,8 V
32	in33	input channel 33 (test channel)			0,8 V
33	Vss_PA	Vss preamplifier (input mirror)	connect to GND	2.05 mA	0 V
34	Ctest_odd	odd channel calibration input	internal Cinjection = 3pF		
35	Vp3	Bias voltage input mirror	to Vdd/GND via 51/56Ω	3,4 mA	2,5 V
36	Vdd_PA	Vdd preamplifier and gain register	connect to Vdd	0,35-3.05mA	5 V
37	Vss_integ	ss integrator before slow shaper	connect to GND	0 to 2,7 mA	0 V
38	V_ref	Reference voltage slow shaper	to connect to pin91	7.5uA	1,2 V
39	Vdd_SS	Vdd slow shaper	connect to Vdd	3,4 mA	5 V
40	Vss_SS	Vss slow shaper	connect to GND	1,7 mA	0 V
41	hold	Hold switch	HI="Track" LO="Hold"		CMOS
42	Vss	Vss connect to GND		≈ 0	0 V
43	out_FS33	output fast shaper CH33	5K series output impedance		2.7 V
44	Vss2_FS	Vss fast shaper (output stage)	connect to GND	1,7 mA	0 V
45	Vss_comp	Vss comparator	connect to GND	3,5 mA	0 V
46	seuil	Comparator Threshold	tuned to Vdc=3V threshold		3 V
47	Vdd_comp	Vdd comparator	connect to Vdd	7 mA	5 V
48	RST_G	gain register reset	active HI		CMOS
49	Q_G	gain register output			CMOS
50	CK_G	gain register clock input	active on positive edge		CMOS
51	D_G	gain register D input	active HI		CMOS
52	RST_R	read register Reset	active HI		CMOS
53	CK_R	read register clock input	active on positive edge		CMOS
54	D_R	read register D input	active HI		CMOS
55	RST_M	mask register Reset	active HI		CMOS
56	Q_M	mask register output			CMOS
57	CK_M	mask register clock input	active on positive edge		CMOS
58	D_M	mask register D input	active LO		CMOS
59	Q_H	Hit register output			CMOS
60	CK_H	Hit register clock input	active on positive edge		CMOS
61	RST_H	Hit register reset	active LO		CMOS
62	Vssd	Vss digital	connect to GND	≈ 0	0 V
63	T	Trigger output	Z_{out} = 1.2KΩ,100Ω external		LVDS
64	Tb	Complementary Trigger output	Z_{out} = 1.2KΩ,100Ω external		LVDS
65	Vddd	Vdd digital	connect to Vdd	≈ 0	5 V

Table 5: *OPERA ROC Pinout (1)*

pin	Name	Description	Comment	Current	DC level
66	vbo_comp	Bias comparator output stage	connect to GND thru 150kΩ	25 mA	3,9 V
67	vbi_comp	Bias comparator input stage	connect to Vdd thru 36kΩ	100 mA	1,5 V
68	vbo_FS	Bias fast shaper output stage	connect to GND thru 36kΩ	100 mA	3,5 V
69	vb_FS	Reference voltage Fast Shaper	to Vdd/GND via 2.2/2.7 MΩ	0	2.75 V
70	vbi_FS	Bias fast shaper input stage	connect to GND via 36kΩ	100 mA	3,5 V
71	vbo_W	Bias Widlar output stage	connect to Vdd via 75kΩ	50 mA	1,3 V
72	vb_CC	Bias Common Collector	connect to Vss via 75kΩ	50 mA	3,6 V
73	vbi_W	Bias Widlar input stage	connect to Vdd via 75kΩ	50 mA	1,3 V
74	SW	Switch T and H Buffer	LO="Widlar", Hi="CC"		CMOS
75	Vbi_SS	bias slow shaper input stage	connect to Vdd via 75kΩ	50 mA	1,3 V
76	Vbo_SS	bias slow shaper output stage	connect to Vdd via 75kΩ	50 mA	1,3 V
77	vb_buf	Bias buffer before slow shaper	connect to GND via 75kΩ	50 mA	3,7 V
78	vb_OTA	Bias for 2 output OTAs	connect to Vdd via 75kΩ	50 mAx2	1,3 V
79	Q	Charge output			1,2V or 2V
80	Vdd_OTA	Vdd output OTA	connect to Vdd	6 mA	5 V
81	Q0	Charge output CH0			1,2V or 2V
82	Vss_OTA	Vss output OTA	connect to GND	6 mA	0 V
83	out_FS0	CH0 fast shaper (threshold ref)	3KΩ series output impedance		2.7 V
84	Vss_comp	Vss comparator	connect to GND	2,125 mA	0 V
85	Vss2_FS	Vss fast shaper (output stage)	connect to GND	1,7 mA	0 V
86	Vdd_FS	Vdd fast shaper	connect to Vdd	6.8 mA	5 V
87	Vss1_FS	Vss fast shaper (input stage)	connect to GND	3,4 to 6,1 mA	0 V
88	Vcc	Vdd protection diodes	connect to Vdd	≈ 0	5 V
89	Vdd_T − H	Vdd sample and Hold	connect to Vdd	5,1 mA	5 V
90	Vss_T − H	Vss sample and Hold	connect to GND	5,1 mA	0 V
91	Vref	Reference voltage slow shaper	to Vdd/GND via 1kΩ/330Ω	7.5μA	1,2 V
92	Vss_SS	Vss slow shaper	connect to GND	1,7 mA	0 V
93	Vss_buf2	Vss buffer before slow shaper	connect to GND	1,7 mA	0 V
94	Vdd_buf	Vdd buffer before slow shaper	connect to Vdd	1,7 mA	5 V
95	Vss_reg	Vss registers	connect to GND	0 mA	0 V
96	Vdd_PA	Vdd preamplifier	connect to Vdd	0,35 to 3.05mA	5 V
97	Ctest_even	even channels calibration input	internal $C_{injection}$ = 3pF		
98	Vss_PA	Vss preamplifier	connect to GND	2.05 mA	0 V
99	in0	input channel 0 (ref. channel)			0,8 V
100	in1	input channel 1			0,8 V

Table 6: *OPERA ROC Pinout (2)*