

Performance of the 32-channels Front End electronic chip

S. Bondil⁽¹⁾, K. Borer⁽²⁾, J.E. Campagne⁽¹⁾, A. Cazes⁽¹⁾,
M. Hess⁽²⁾, Ch. de La Taille⁽¹⁾, A. Lucotte⁽¹⁾,
G. Martin-Chassard⁽¹⁾, L. Raux⁽¹⁾, J.P Repellin⁽¹⁾

⁽¹⁾ LAL-IN2P3 - Univ. Paris-Sud - B.P. 34 - 91898 Orsay Cedex

⁽²⁾ Bern University, Bern, Switzerland

Abstract

Multi-anode photomultipliers HM7546 are used to readout signal from the OPERA Scintillator Tracker[1]. A 32-channels front-end chip prototype accomodating the HM7546 has been designed at LAL. Test board and test equipement for the FE chip have been designed and constructed by the Bern group. Both institutes have undertaken series of tests for validation. We report here the results of the tests performed by both groups on the FE chip. Special emphasis is put on the characterization of the variable gain preamplifier, auto-trigger and charge measurement functionalities.

A single-channel test chip has also been designed with new features aiming at improving some aspects of the 32 channel chip. Results of performed tests are reported in details and their impact on the chip performance is estimated. Finally, plans for future versions are discussed and a new schedule leading to mass production for the Target Tracker is proposed.

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1 Scintillator Tracker requirements

The first version of the 32-channels chip was defined to accommodate multi-anodes Hamamatsu H7546 PhotoMultiplier Tubes (PMT). These PMT's are required to function with a global gain of "a few 10^5 ", with gain excursion not exceeding a factor 3 among the 64 channels, as defined in the supply contract [2]. The LAL shares the responsibility with Bern University to provide the front end electronics for the 992 PMT's used to readout signals from the scintillator Target Tracker of OPERA. While LAL designs the ASIC's used to readout signal from the scintillator Target Tracker, Bern university designs the mother Boards that implement the FE chip. The requirements, set by physics and technical constraints, are the following:

- a variable gain preamplifier with the capability to correct for channel-to-channel gain variations as high as 300%. Studies already performed on Hamamatsu H7546 PMT's show that such level of correction is needed [3]. The preamplifier amplifies the various PM channel gain to be seen by both slow and fast channels *as if they were all at gain 10^6* .
- an auto-triggering system 100% efficient down to a few 1/5th of photoelectron *at each end of a strip*. This is defined by the need to detect particles going through the detector at the minimum of ionisation (mip), which has been measured at 6.6 (5.0) photoelectrons [4];

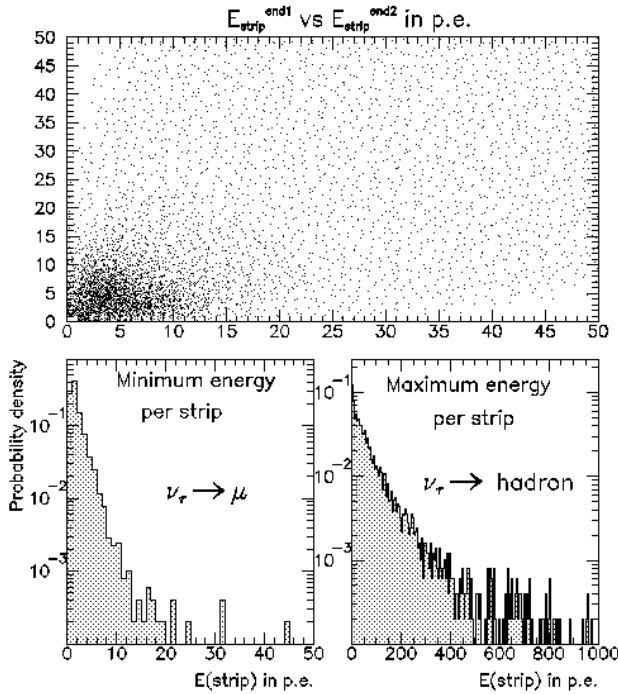


Figure 1.1: *Dynamic range of two physics processes of interest. The top figure displays the energy per strip as measured by both ends; bottom plots show respectively the minimum and maximum energy deposited per strip and per end for $\nu_\tau \rightarrow \mu$ and $\nu_\tau \rightarrow \text{hadron}$. All numbers are in photoelectron*

- a charge measurement system reliable over a dynamic range defined between a few 1/5th of photoelectron to a few 100 photoelectrons, which corresponds to the physics input range.

In only a small fraction of events higher energy depositions are measured in a single strip as seen in Fig. 1.1, for which the energy measurement is not considered as crucial as for lower values;

- a multiplexed output including the autotrigger, the time and charge measurements for each channel; although not a strong requirement, readout must function at a rate of 5 MHz. Also a masking of noisy channel(s) has to be provided.

2 Performance of the 32-channel chip for multi-anode PMT

Chip performances have been measured using a test card and test equipment designed and constructed by Bern University. No real PMT pulse has been injected yet and all tests are done with electronic charge injection through a 4.7 pC capacitor. Similar tests of the chip have been conducted in parallel by both the LAL and the Bern groups. A view of the 32 channel chip is shown in Fig.2.2.

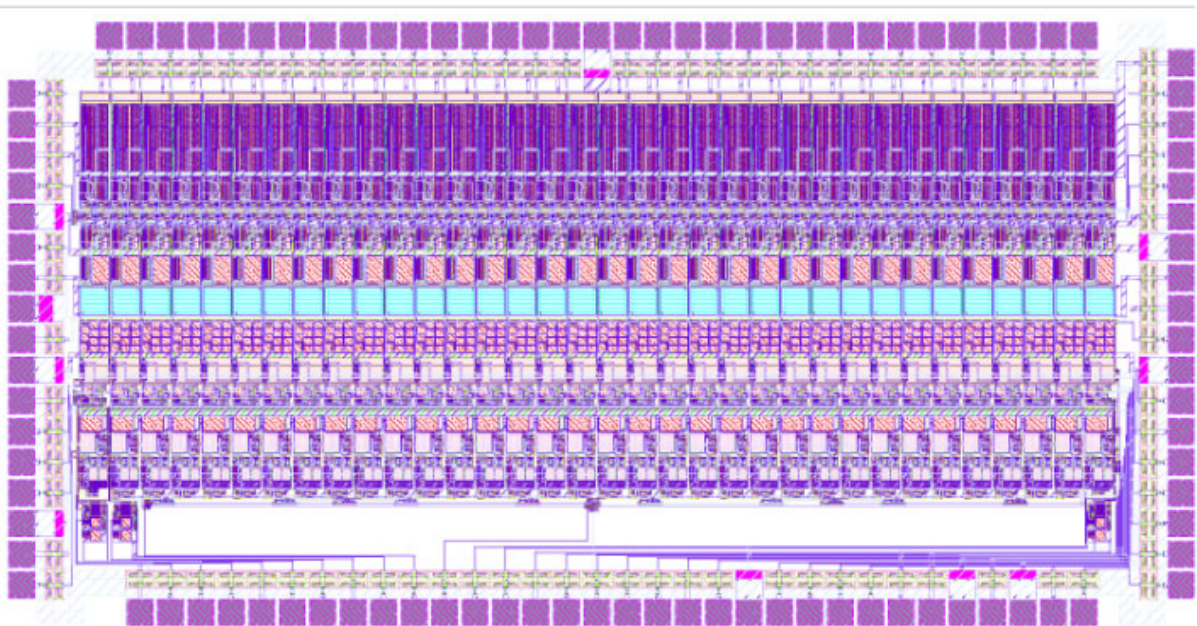


Figure 2.2: *View of the 32 channel chip design. Total area is about 10 mm²*

2.1 Chip Design and main features

Based on the AMS 0.8 μ m BiCMOS technology, a complete chip with 32 channels and 2 extra test channels has been designed by the LAL group to fulfill the Target Tracker requirements. The chip architecture includes a variable gain preamplifier, based on a current mirror architecture; an

auto-trigger channel including a fast shaper followed by a comparator; and a charge measurement channel, with a slow shaper and an (on-chip) Track and Hold structure. An output multiplexer is then used to rout the signal out with a readout frequency of 5 MHz. Schematics of a single channel is displayed on Fig. 2.3.

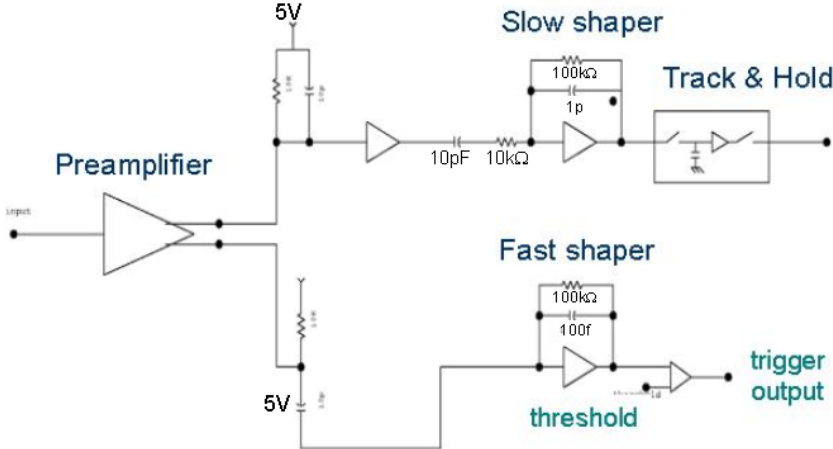


Figure 2.3: Single channel schematics for the 32-channel chip designed at LAL to readout multi-anode PhotoMultiplier

The chip comprises 32 such channels (channel 01 to 32) with individual inputs, trigger, and charge measurement. Channel 33 is powered separately and is designed to provide intermediate outputs for thorough examination of the signal integrity. In the following, most figures displayed are taken from measurements performed on Channel 33, except when explicitly specified. Note that with a PMT gain of 10^6 , 1 photoelectron (p.e.) corresponds to 160 fC, value that will be used hereafter as conversion factor.

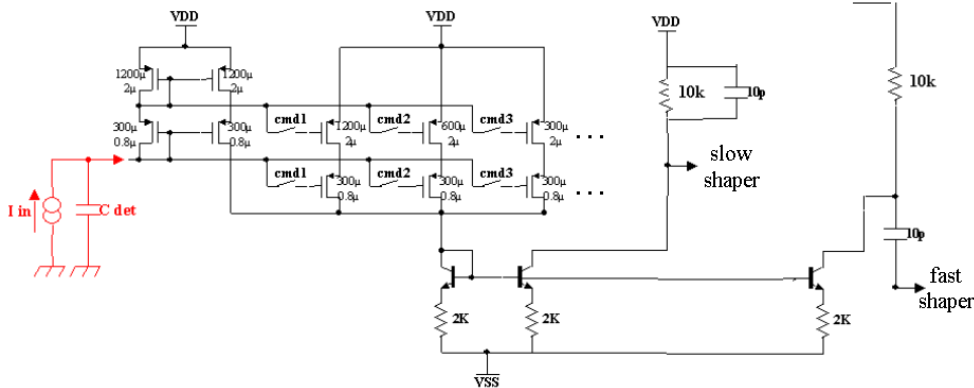


Figure 2.4: Variable gain Preamplifier schematics for every individual channel. $cmd1$ to $cmd4$ are the switches that (dis)enable the current correction. Time constant for signal is set to 100 ns.

2.2 Preamplifier measurements

The preamplifier is based on a current mirror architecture, with ratioed mirrors on input and output currents summed and integrated on a 10 pF capacitor [5]. The schematics of the preamplifier is shown on Fig. 2.4. The input impedance is about 1.5 k Ω , while the time constant is set to 10 k Ω \times 10 pF = 100 ns.

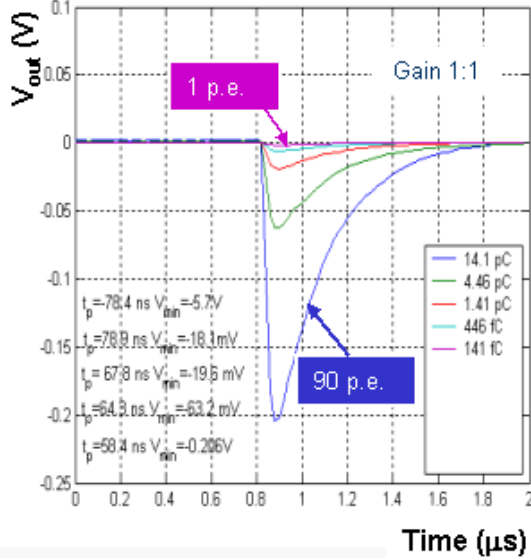


Figure 2.5: Preamplifier Output waveform for different input charges in Channel 33

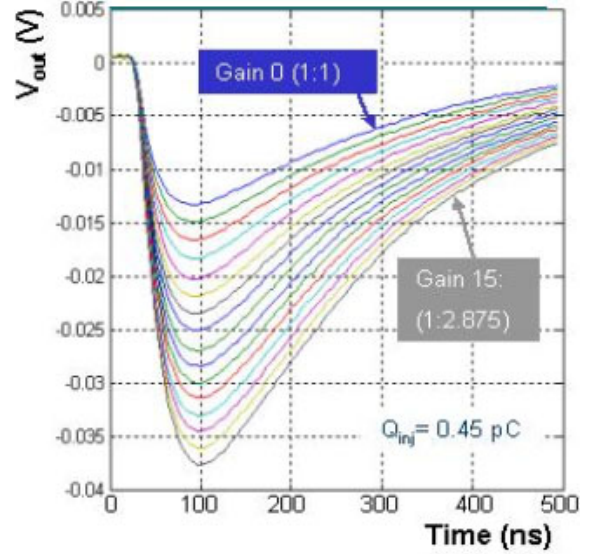


Figure 2.6: Preamplifier output waveform for different gain correction settings in Channel 33

The gain correction is adjusted via the use of four mirror “switches” (loaded through registers) located on the test card, with respectively 1, 1/2, 1/4 and 1/8 times the input current. A maximum correction factor of 2.875 can thus be obtained with all switches “on” with a small step of the correction of 12.5%. Preamplifier gain has been measured for all channels. Gain is found to be 25 mV/pC (4 per p.e.) for Channel 33 and about 60 mV/pC (9.6 per p.e.) for Channel 1 to 32, as shown in Fig.2.5 for a null gain correction. The difference in gain between Channel 33 and the others is due to parasite external capacitance from the test board coming in parallel with the 10 pF of the Channel 33 preamp output.

All levels of gain corrections have been applied to an input signal corresponding to about 1 p.e. Fig.2.6 shows the waveform as measured in channel 33 for the whole set of gain correction. The use of the 4 bits sets 16 possible levels of correction that are proved to be reliable over the whole range. Residuals remain below 1% of the correction level over the full range of correction. A small degradation of these performance has been seen for channels 01 to 32 due to parasitic resistance in the power distribution among the 32 channels. This effect will be cured by redistributing power supplies in the next chip iteration, Version 1a.

2.3 Auto-trigger channel measurements

Both fast and slow shapers have been designed according to a classical CRRC architecture. The fast shaper schematics is shown in Fig. 2.7. Resistor and capacitor values are chosen to set relevant peaking time and gains. The common-emitter plus common-collector amplifier provides an open loop gain of 560 and a bandwidth of 3.5 GHz. Power dissipation of 1 mW is measured.

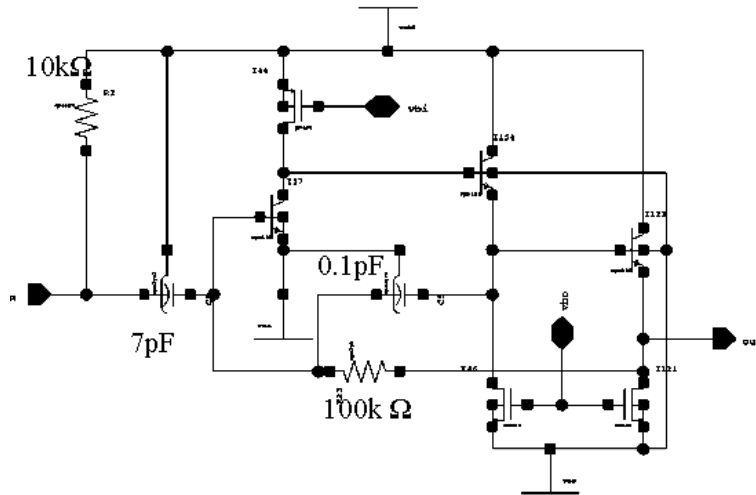


Figure 2.7: Schematics of the Fast Shaper

For all channels, the gain is measured at 800 mV/pC (130 mV per photoelectron). The peaking time is about 30 ns and is quite independent of the charge input, as seen in Fig.2.8.

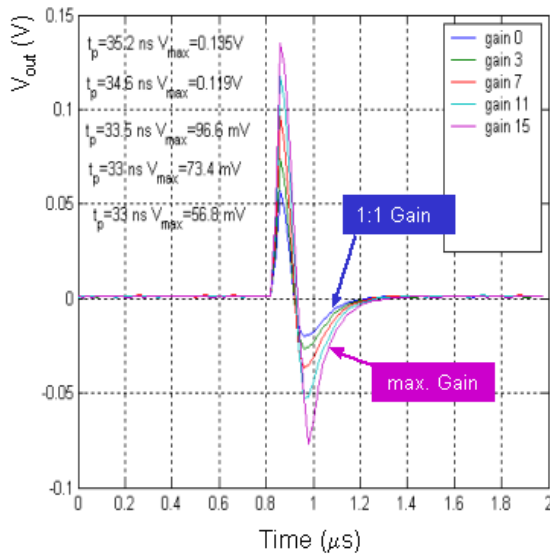


Figure 2.8: Output waveform measured at the Fast Shaper (Ch33) for a set of gain correction ranging from 1 to 2.875

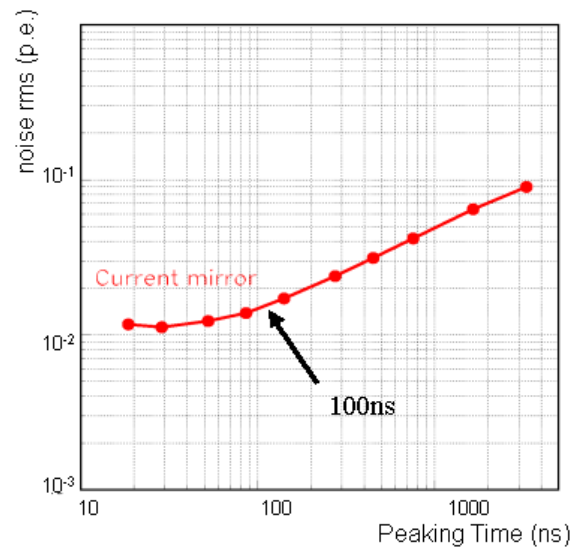


Figure 2.9: (Charge equivalent) Noise RMS in photoelectron as measured for the shapers. Slow shaper functions at 30 ns, fast shaper at 100 ns

Electronic noise has also been measured using an external shaper, with adjustable peaking time by measuring the distribution of pulse heights for a fixed charge injected to the input. The charge equivalent noise is then given by $ENC = Q_{inj} \times \frac{\sigma_{(rms)}}{V_{max}}$. Noise is found to remain below 1% of p.e. at $t_p = 30$ ns corresponding to the fast shaper, as shown in Fig.2.9. It therefore appears negligible.

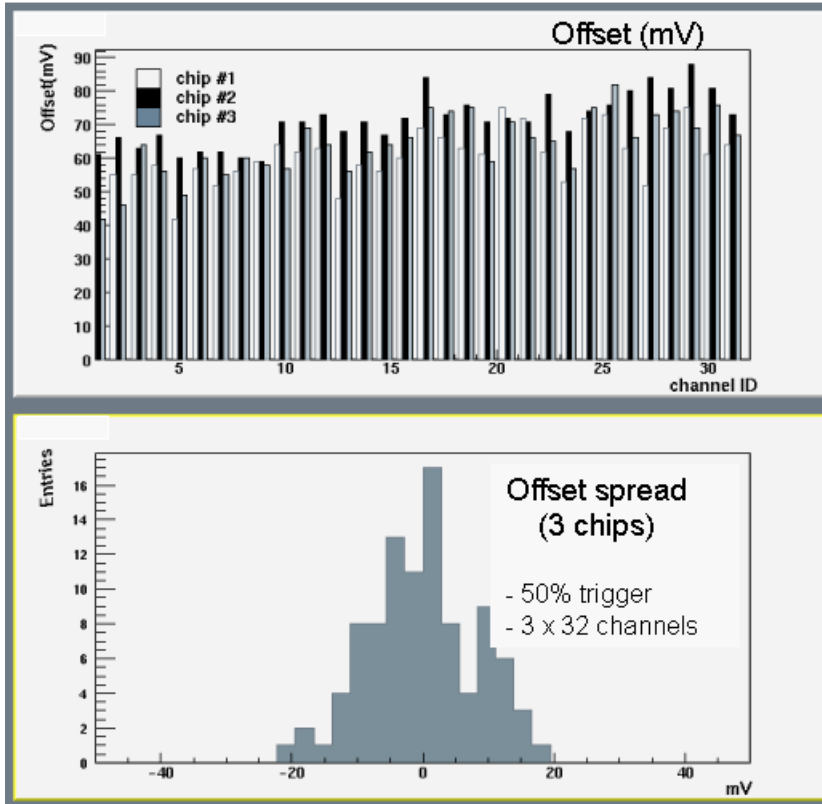


Figure 2.10: *Relative Offset (peak-to-peak) in mV measured on the 32 channels. The spread is about 70 mV, ie about 1/2 photoelectron*

Pedestal measurements on the 32 channels show a spread of about 70 mV peak-to-peak if one conservatively requires a 100% trigger efficiency. This corresponds to about 1/2 photoelectron. This spread is measured at about 30 mV if with a 50% trigger efficiency requirements on three different chips, as shown in Fig.2.10 (Trigger efficiency is measured by setting the threshold to a fixed value and applying a variable input charge to the measured channel until no trigger output is measured). This spread is mainly due to the Fast Shaper. The comparator contribution is estimated at around 1 mV and is negligible compared to the latter.

The current pedestal spread and comparator problems reduce the ability to trigger for all channels at a fraction of p.e. Comparator has a few design problems coming from a common supply for analog and digital parts. The output inverter is too large and sizeable resistors are present in the current design. This results in an unacceptable over-current that necessitates external had-oc fixes to make it work. This flaw will be corrected in the next version of the 32-channel chip, Version 1a.

2.4 Charge measurements

Slow shaper design is similar to the fast shaper one. Schematics is shown in Fig. 2.11. The common-emitter plus common-collector amplifier provides an open loop gain of 540 and a bandwidth of 5.0 GHz. Power dissipation of 0.5 mW is measured. The slow shaper is followed by a Track & Hold architecture, which is based on CMOS switches with transistors to compensate the injected charge. The maximum of the slow shaper signal is stored in a 2 pF capacitance.

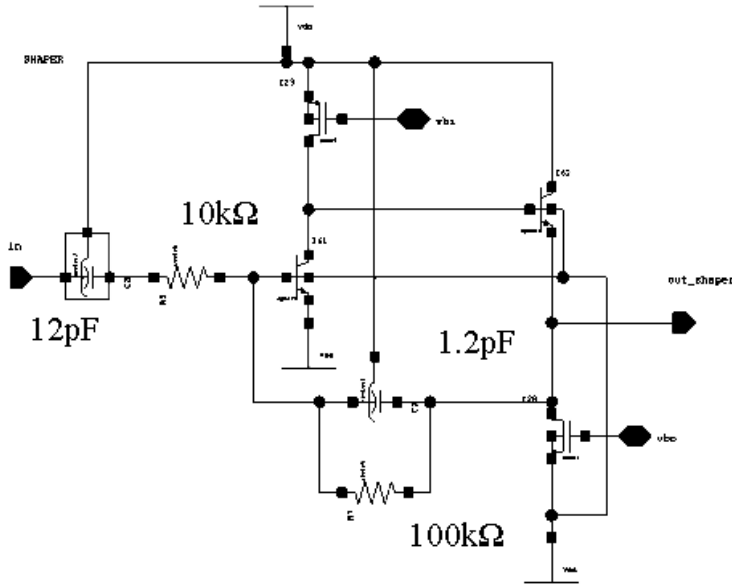


Figure 2.11: *Layout of the 32 channel chip slow shaper*

Gain and peaking time have also been measured. Channel 33 gain is measured at 100 mV/pC (15 mV per p.e.) while channels 01 to 32 have a gain of about 170 mV/pC (27 mV per p.e.). Peaking time is 130 ns for Channel 33 and about 100 ns for the others, as shown in Fig.2.12. Differences in the results seen between channel 33 and the others are understood. They are due to the fact that for Channel 33, output signal is measured externally and is thus sensitive to external capacitors and resistors (cable).

The response linearity has been measured as function of the input charge from 0 to 80 photoelectrons and no deviation is seen above 1% over the full range, as shown in Fig.2.13. The Track and Hold has also been tested and found fully operational.

Pedestal measurements on the 32 channels show a spread of 40 mV peak-to-peak, which corresponds to about 1 photoelectron. This pedestal spread comes from two identified sources, about 50% from the slow shaper, and 50% from the Track & Hold buffer. Fig.2.14 displays the relative offset peak-to-peak as measured for the 32 channels for a correction gain fixed at 1 (no gain correction). This channel to channel spread may be taken care of by offline corrections. It is however possible to improve the design of both slow shaper and Track & Hold to reduce pedestal offsets.

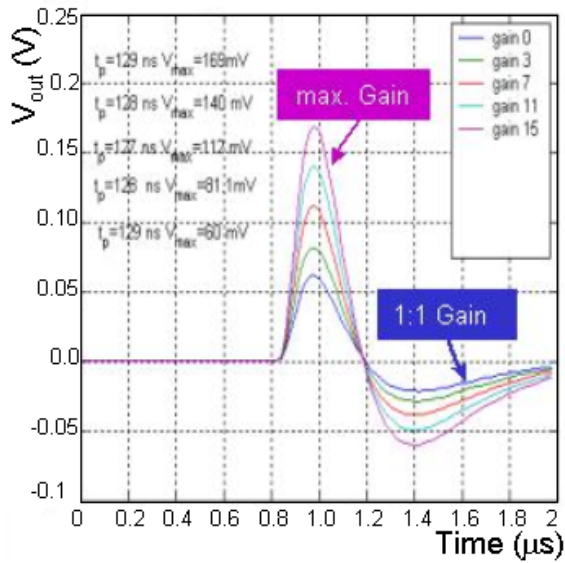


Figure 2.12: *Slow shaper Output waveform for a set of gain correction*

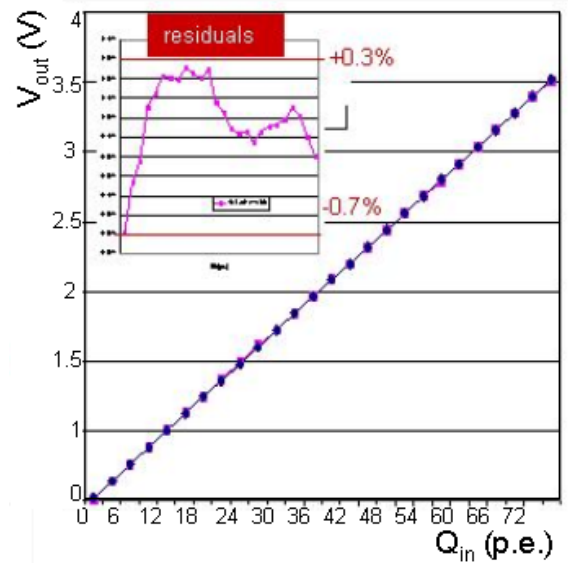


Figure 2.13: *Slow shaper linearity as function of input charge in unit of photoelectron*

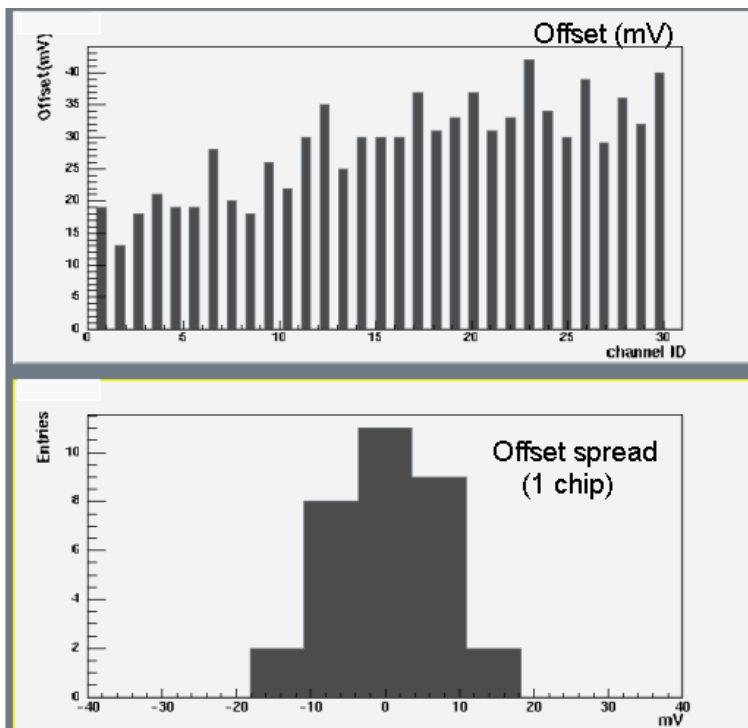


Figure 2.14: *Offset (peak-to-peak) in V measured on the 32 channels. The spread is about 40 mV, ie about 1 photoelectron*

Regarding the noise, the measurements have been detailed in the Section 2.3.1. and shown in Fig.2.9. Noise is about 2% for the slow shaper, and therefore appears negligible.

2.5 Multiplexing and Mask

Test results performed at Bern and LAL show no problem. The output level is around 3V for the maximum amplitude. In the present design, noisy channel cannot be switched OFF. Instead, there is a mask at the trigger level (AND after the comparator) that allows to avoid triggering on the noisy channel. The readout is clocked at 5MHz and it takes $6.4\mu\text{s}$ to read the 32 channels (in serie).

2.6 Cross-talk

Fig.2.15 displays the waveform output of a channel with an injected charge of 0.45 pC compared to the one of an adjacent channel. The present measured channel-to-channel cross-talk is of the order of 2% and is mainly due to the high level of input impedance of the preamplifier.

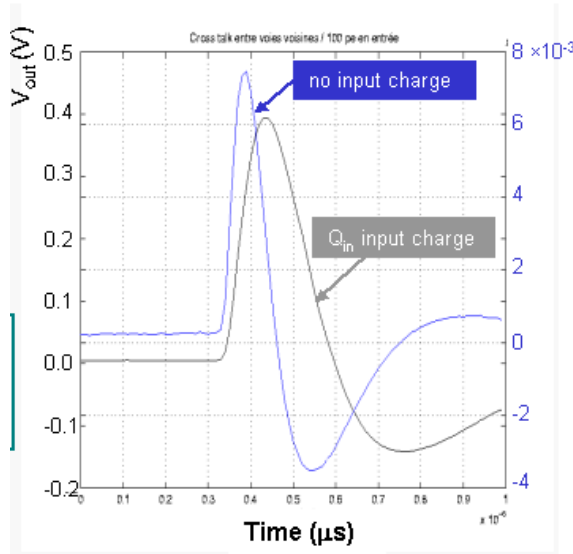


Figure 2.15: Cross-talk measured between two adjacent channel. Grey waveform corresponds to the channel with a 0.45 pC injected charge while the black waveform is the adjacent channel output

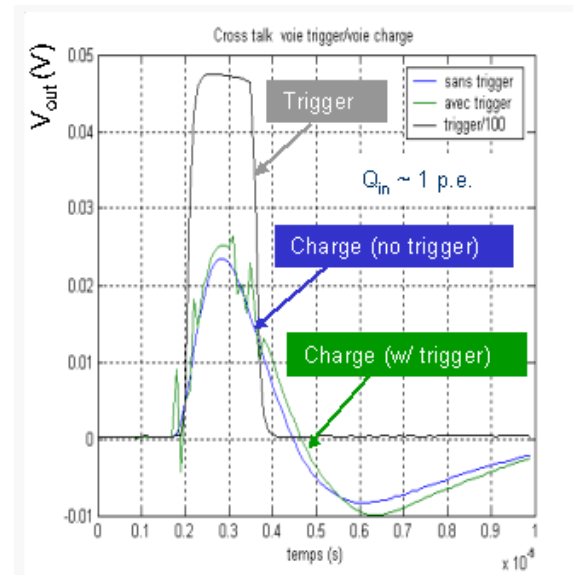


Figure 2.16: Observed cross-talk between the trigger and an output measured after the Track and Hold buffer

Another cross-talk effect is seen between the trigger and the charge measurement channel as seen on Fig.2.16. The digital signal (0-5V logic) produced by the comparator on a given channel produce by coupling a signal on the charge measurement of other channels (even if themselves they have no input signal). It amounts approximatively to an increase of about 4 mV (0.1 p.e) when all the channels have an input signal, and this offset is independant to the input signal level. This additionnal peak up signal seems to be a coupling between the comparator output

and somewhere after the preamplifier as this phenomenon is independant of the weights applied to the channel with no input. One notices also some influence due to the mask of the channel which receives the input signal. The exact origin of the coupling is probably due to power supply glitch to the comparator.

2.7 Summary

Table 1 reports the performance as measured on the 32 channel chip. Except for the comparator over-current that necessitated an “had-oc” fix to function normally, the chip performance suits the Target Tracker requirements. A 100% trigger efficiency is ensured down to 1/2 photoelectron and the linearity in the charge measurement is ensured in the [1-80] photoelectron range. The next version of the chip (Version 1a) is a replica of this one except for the change in the comparator design, which should cure the overcurrent problem. This Version is considered as the fallback version for future developpments.

A second iteration of the chip could however include new features in order to improve the performance in terms of pedestal spread, threshold spread and cross-talk. These new features have been tested on the “mecano” chip presented hereafter.

Auto-Trigger: - Fast shaper peak time - Fast shaper Gain - Pedestal Spread - Noise RMS - Comparator Threshold(*)	$t_p = 35 \text{ ns}$ 800 mV/pC (130 mV/p.e) 30 mV (50% trigger) 1.5 mV ($\ll 1 \text{ pe}$) 1/2 pe
Charge Measurement: - Dynamic range - Slow shaper peak time - Slow Shaper Gain - Pedestal Spread - Noise RMS - Gain Correction - Track & Hold - Cross-talk	[0-13 pC] (80 p.e) $t_p = 100 \text{ ns}$ 100 mV/pC (16 mV/p.e) 80 mV (5 p.e.) 0.5 mV (3% p.e.) 1 to 2.875 (4 bits) Operational $\mathcal{O}(2\%)$
Multiplexing Clock frequency Mask of noisy channel Trigger signal Tag of the triggered channel	Operational (3V max. output) 5 MHz (6.4 μ s/32channels) Trigger Level Comparator output Not included

Table 1: *Functionalities of the 32-channel chip. (*) : once the overcurrent problem solved externally*

3 Performance of the mecano chip

Characteristics of the 32 channel chip are found to suit the Target Tracker requirements. However, the fast shaper (trigger) shows offset variations of about $1/2$ photoelectron, while slow shaper and Track & Hold buffers offsets cause variations as high as 2-5 photoelectron in the charge measurements. This is the main motivation to test other designs, such as the ones implemented in a single channel test-chip, called the “Mecano” chip. This chip has been produced in parallel to the 32-channel chip, and includes a set of special features that are expected to bring significant improvements in the pedestal spread, cross-talk and dynamic range.

3.1 Chip Design and main new features

Based on the AMS $0.8\mu\text{m}$ BiCMOS technology, single-channel chip have been designed by the LAL group to test some new features. The chip architecture includes a new variable gain preamplifier with lower input impedance. It also comprises a new low-offset fast shaper, followed by a comparator similar to that used in the 32 channel chip, as well as a new low-offset slow shaper. Finally, a new feedback Track and Hold structure is also implemented. A view of the single channel chip is displayed Fig. 3.17.

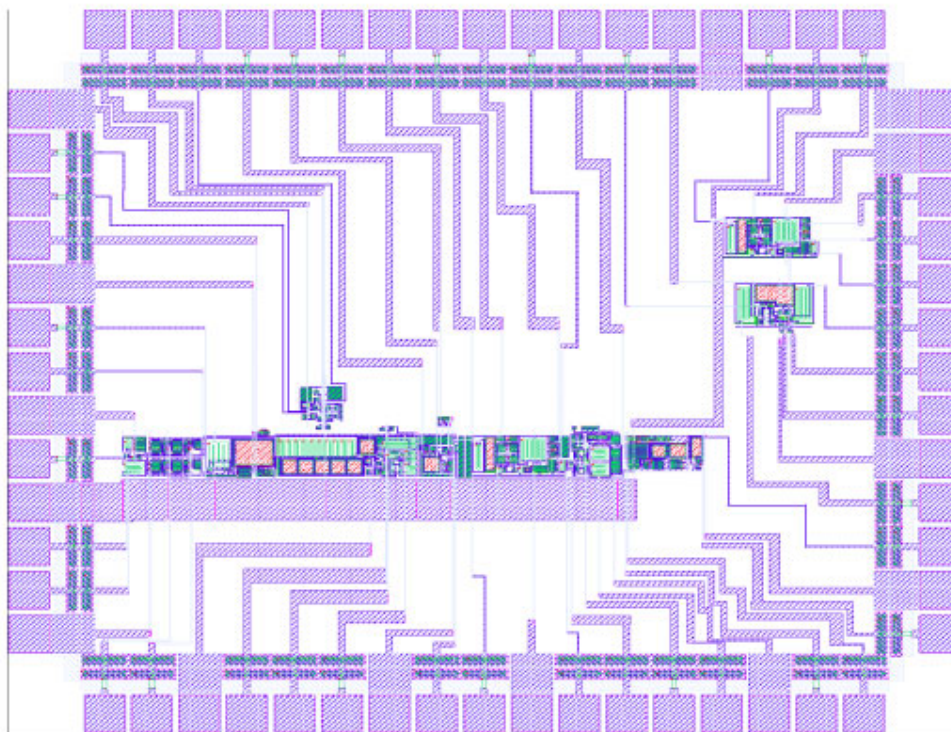


Figure 3.17: *View of the Mecano (single channel) chip design, with a low impedance preamplifier and new featured shapers*

3.2 Preamplifier measurements

A new preamplifier has been designed with a “super common base” input stage that includes a lower input impedance of 70Ω , compared to the $1.5 \text{ k}\Omega$ in the 32 channel case. This new structure decreases the input impedance so that the current in the mirror can be divided by a factor 4 (from 100 to $25 \mu\text{A}$). The preamplifier principle and schematics are illustrated in Fig. 3.18. Input impedance is shown as function of current I_{DC} on Fig. 3.19.

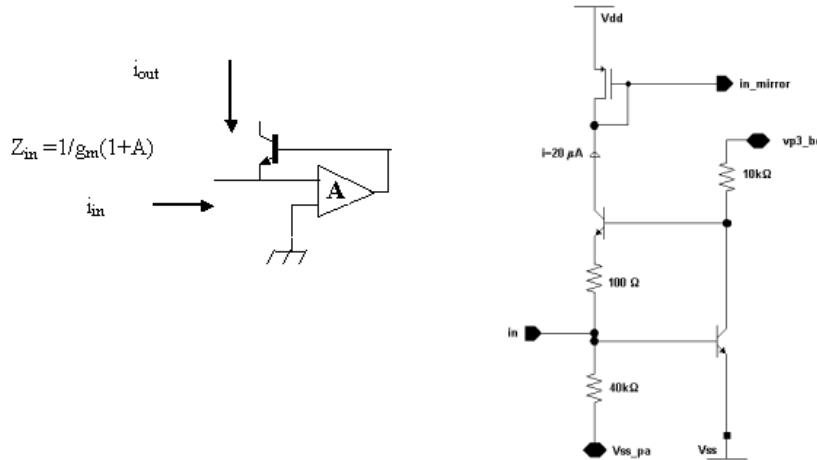


Figure 3.18:
 (left) Principle of the “Super common base” architecture
 (right) Schematics of the new variable gain preamplifier

The preamplifier design is based on a current mirror architecture similar to the preamp used in the 32 channel chip. In this device however, the architecture includes only two mirrors with a weight of 1 and 0.5 times the input signal for a maximal gain of 2.5.

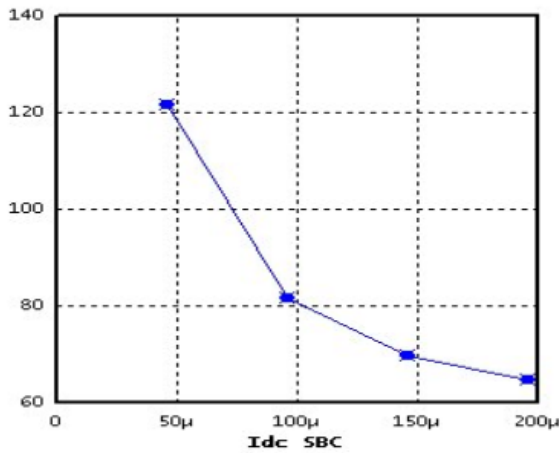


Figure 3.19: Input Impedance Z_{in} as function of I_{DC}

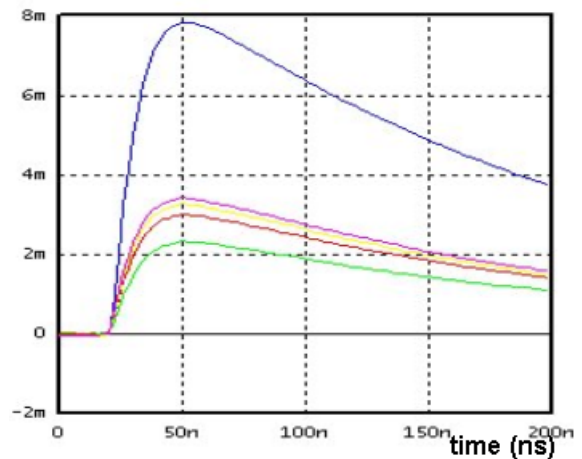


Figure 3.20: Preamplifier output waveforms measured for different input charges

All levels of gain corrections have been successfully tested and Fig.3.20 shows waveforms mea-

sured for different input charge going from 1/3 of a photoelectron to 300 photoelectrons.

3.3 Auto-trigger measurements

In the test chip, both fast and slow shapers designs are based on a differential pair of amplifiers. This differential configuration provides a way to reduce drastically the offset (to 0 at the 1st order) to levels well below 1%. This architecture is used for both the fast and slow shapers, and is described in Appendix B, which displays the fast shaper layout. Fig.3.21 displays fast shaper output waveforms for different input charges. Peaking time is measured to range between 20-25 ns with a gain of 1.5 V per pC (250 mV per p.e.).

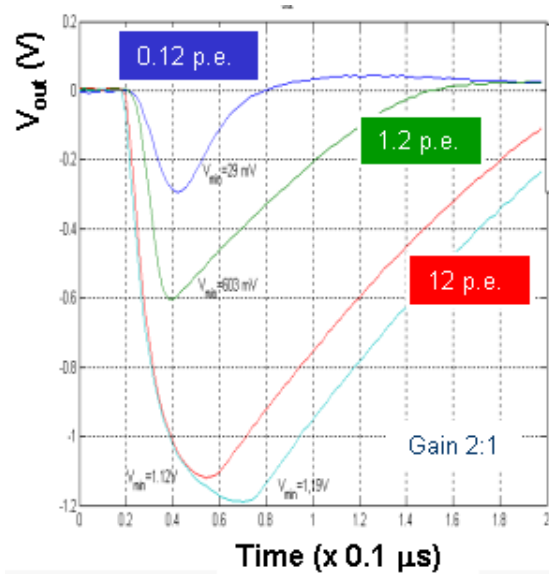


Figure 3.21: Fast shaper output waveforms for different values of input charge

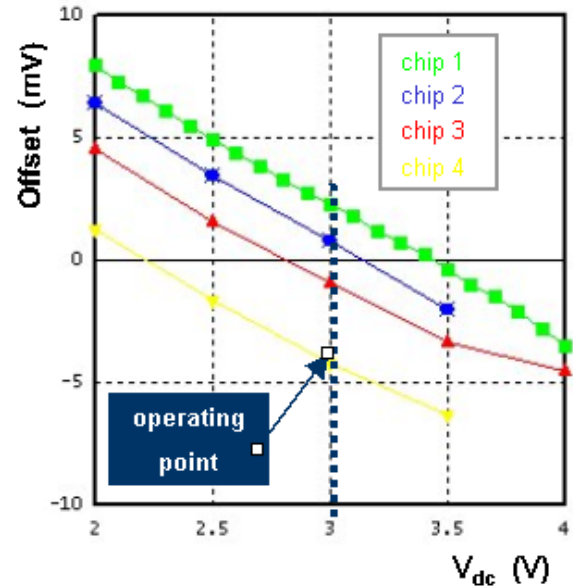


Figure 3.22: Fast shaper spread as measured with four different single-channel chips

Peak-to-peak pedestal spread of ± 3 mV has been measured on four independent single-channel chips, as shown in Fig.3.22. This result represents a gain of a factor of 20 with respect to the previous 32-channel standard configuration and constitutes the most pessimistic view compared to measurements that would be performed on channels from the same chip.

Noise has been measured for two gain corrections: for a null gain correction, the noise RMS is measured at $420\mu\text{V}$, while for a 2.5 gain, noise RMS remains around $850\mu\text{V}$. This noise level therefore appears completely negligible.

3.4 Charge measurements

Characteristics of the slow shaper have been determined. Peaking time has been increased compared to the 32 channel chip to a value of about 190 ns in order to be less sensitive to fluctuation. Gains are found at 63 mV/ pC (10 mV/ p.e.) for a null gain correction and

160 mV/pC (25 mV/ p.e.) for the maximum correction (2.5).

As for the slow shaper, the DC pedestal has been measured on four independent chips. Results are reported in Fig. 3.24 and show that the spread is well below 1 mV. Again, this represents a pessimistic case and we expect that the results from channel to channel measurements in a single multichannel chip should be below this level. This value corresponds to an improvement by a factor of 40 with respect to the present 32 channel design. The slow shaper response is linear within 1% over a dynamic range of 0-300, as shown in Fig.3.23. It is however clear that if linearity is not needed for input charge above 100 pe, linearity is a strong requirement for lower values.

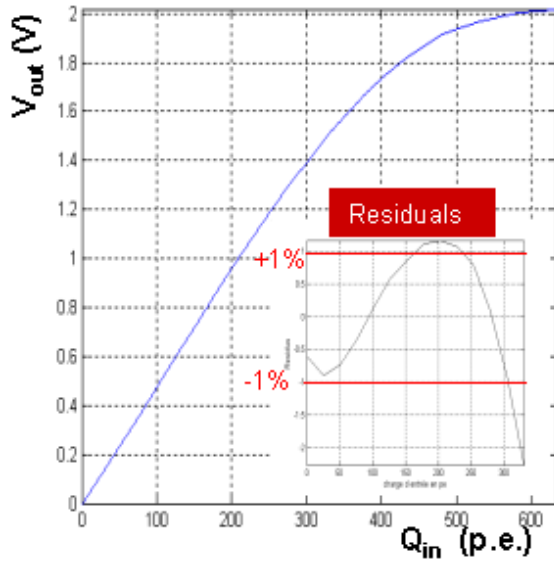


Figure 3.23: *Slow shaper output linearity as function of input charge*

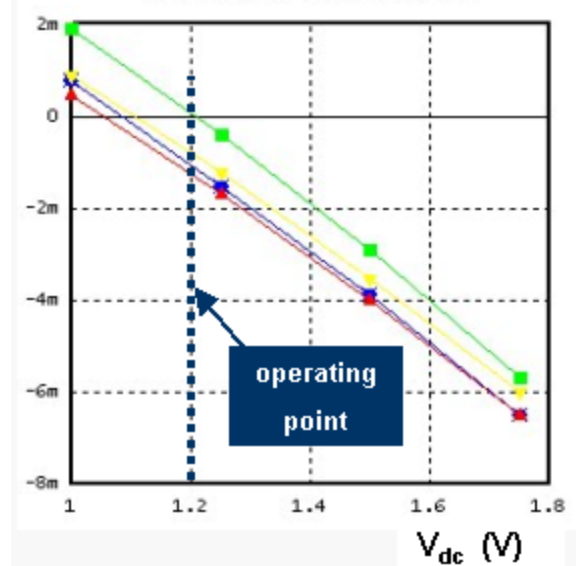


Figure 3.24: *Slow shaper spread as measured with four different single-channel chips*

Noise RMS is measured at $800\mu\text{V}$, which, similarly to the fast shaper measurements, appears negligible compared to spread values.

3.5 Summary

Two main features are tested with the Mecano chip. A new configuration, based on differential pair of amplifiers, is included in both the fast and slow shaper. Tests are very conclusive since measurements show a drastic reduction in the shaper offsets by a factor 20 to 40 compared to the 32 channel chip. This represents a significant improvement in terms of precision for low signal threshold settings as well as pedestal spread.

A low input impedance preamplifier is used. This design has been tested and proven reliable. We expect this configuration to reduce cross-talk to negligible level compared to the 2% measured in the 32 channel chip. Both features thus appear very promising and will be implemented into

the Vers. 2 design. Table 2 reports the results of all measurements performed on the two chips.

	32 channel	“Mecano” 1-channel
Auto-Trigger: - Fast shaper peak time - Fast shaper Gain - Pedestal Spread - Noise RMS - Comparator Threshold	$t_p = 30$ ns 800 mV/pC (130 mV/p.e) 30 mV (50% trigger) 1.5 mV ($\ll 1$ pe) 1/2 p.e.	$t_p = 20$ ns 1.5 V/pC (250 mV/p.e) 4 mV 500 μ V –
Charge Measurement: - Dynamic range - Slow shaper peak time - Slow Shaper Gain - Pedestal Spread - Noise RMS - Gain Correction - Track & Hold - Cross-talk	[0-13 pC] (80 p.e) $t_p = 100$ ns 100 mV/pC (16 mV/p.e) 80 mV (5 p.e.) 0.5 mV (3% p.e.) 1 to 2.875 (4 bits) Operational $\mathcal{O}(2\%)$	[0-300]p.e. $t_p = 190$ ns 65 mV/pC (10 mV/p.e.) <1 mV 0.3 mV 1 to 2.5 (2 bits) Operational –
Multiplexing Clock frequency Mask of noisy channel Trigger signal Tag of the triggered channel	Operational (3V max. output) 5 MHz (6.4 μ s/32channels) Trigger Level Comparator output Not included	

Table 2: *Compared performance of the 32-channel chip and the Mecano chip*

4 Plans and schedule

The present 32-channel FE chip is close to suit the Target Tracker requirements, except for the unreasonably high over-current in the comparator, see Section 2. The tests made in parallel on the Mecano chip showed that the differential configuration brings substantial reduction of pedestal spread (factor more than 20) and that a reduced impedance preamplifier should decrease the cross-talk significantly, see Section 3.

4.1 Corrected Design: Version 1a

Version 1a does not include any significant change in the chip layout with respect to the chip tested in this study. The only modification concerns the new design for the comparator, now including a new power supply distribution, new resistors and a smaller inverter. No other change in the design is made. For completeness, the design of the comparator for Vers. 1a is given in Appendix A.

Version 1a design has been submitted 27 September 2002 and the chip should be available for testing January. This version actually constitutes the fallback version for the FE ASIC and is pin-to-pin compatible with Vers.1 so that it can be tested with the same test setup.

4.2 Improved Design: Version 2

Version 2 is an improved version of the 32 channel chip and has been submitted Nov. 15th for production. It includes all new features already tested in the mecano chip duplicated for all 32 channels. That is reduced impedance preamplifier and low differential fast and slow shapers. Preamplifier will also provide an extended range of correction, with 5 switches allowing to add 2, 1, 1/2, 1/4 and 1/8 times the current to the input signal. A 6th bit will be used to turn off / on completely the channel, providing an easy (and redundant) way of masking a dead channel. In the previous version, masking only took place at the trigger level.

Regarding the auto-trigger channel, a differential fast shaper will be implemented and the Vers. 1a comparator will be used. The fast channel should thus benefit from the strong reduction in pedestal spread. The new spread value is expected well below 1% of a photoelectron, which suits well the Target Tracker requirement.

As for the charge measurement channel, both a new slow shaper and a new Track & Hold architecture will be implemented in the chip. A differential slow shaper should allow to reduce offset spread by about half of the present value, that is about 40 mV. However, in order to fully benefit from such improvement in the charge measurement, the Track and Hold architecture must be improved. Indeed, in the present 32 channel chip, Track & Hold buffer accounts for about 50% of the total spread. It is thus foreseen to implement a new and improved structure, also making use of the differential configuration. However, to make sure that the Version 2 chip is as close as possible of the final design, Verion 2 chip will also conservatively include the present 32 channel

Track & Hold structure which has been proven reliable. The choice among the two options is ensured by the use of a switch set for every channel. The implementation of both solutions does suit the present size of the chip. Version 2 Track & Hold design is shown in Appendix E.

Regarding Version 2 schedule, the design submission has been made on November 17th and the production is expected to be completed four months later, in early april 2003. A period of two months of testing is then needed to validate the chip. These tests should include real PMT's signals to debug all or part of the readout chain, from the PMT to the ASIC's, the mother and readout boards. Decision for full production should be taken around July 2003, and implies a choice between the fallback Version 1a or the Version 2 chip.

4.3 Costs estimates

The cost for a multiproject including 15 units (produced, packed and encapsulated) is ≈ 5.2 kEuros. This estimate is basically unchanged from Version 1a to Version 2 since it mainly depends on the chip area, which remains basically identical. The cost estimate for a full production based on 2000 ASIC's is about 46 kEuros. All numbers are reported in Table 3.

	Nb of ASIC units	Cost per channel	Total Cost
Version 1a (test)	15	10.8 euros	5.2 keuros
Version 2 (test)	15	10.8 euros	5.2 keuros
Version 2 (full prod.)	2000	0.7 euros	46.0 keuros

Table 3: *Cost of the ASICs designed by the LAL group*

A Version 1a & 2: Layout of the comparator

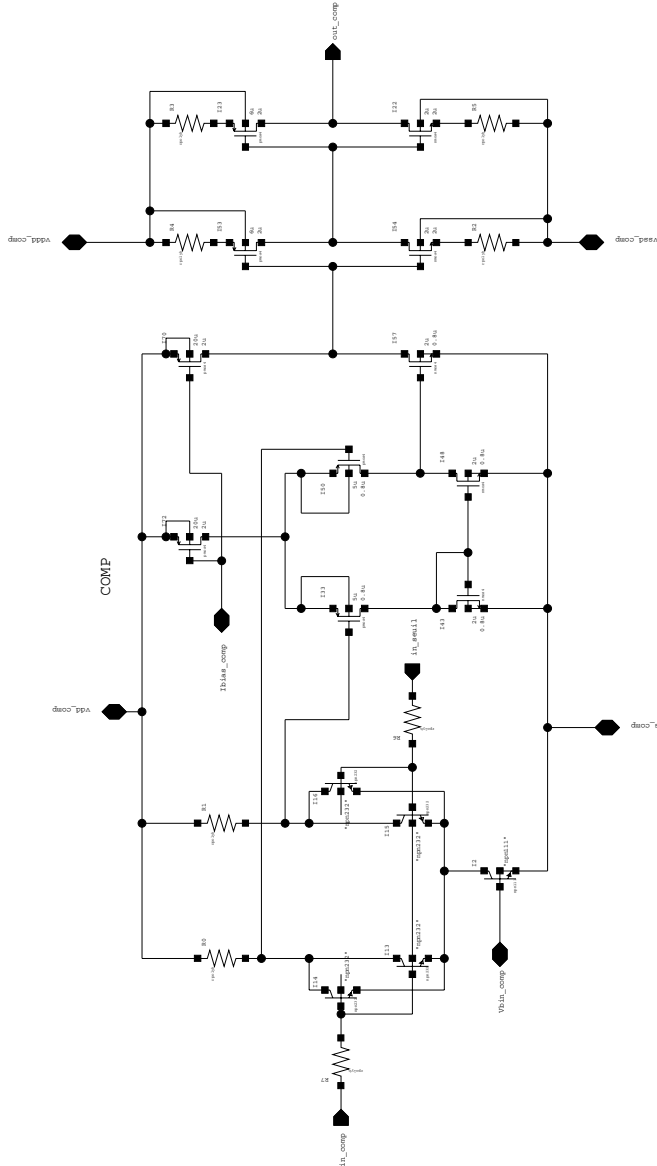


Figure A.25: Layout of the comparator designed in Version 1a

B Version 2: Layout of the fast shaper

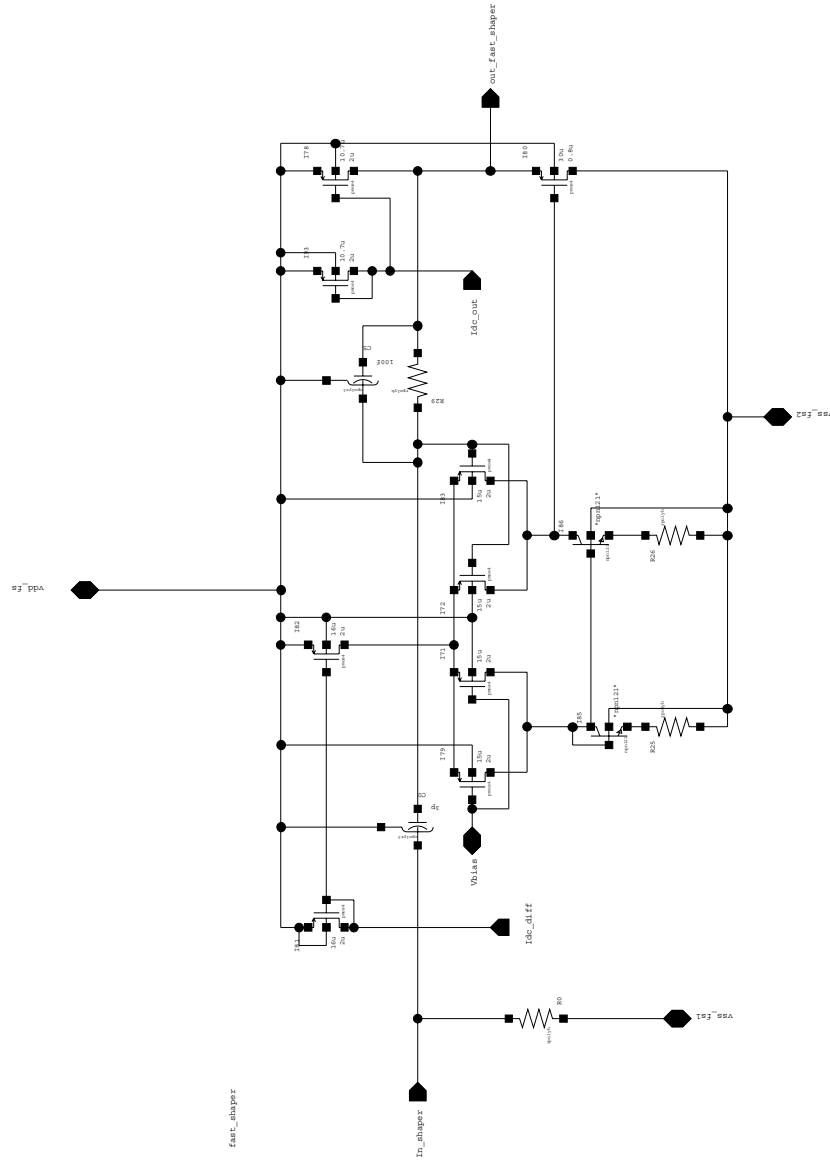


Figure B.26: Layout of the Fast Shaper designed in the mecano Chip

C Version 2: Layout of the slow shaper

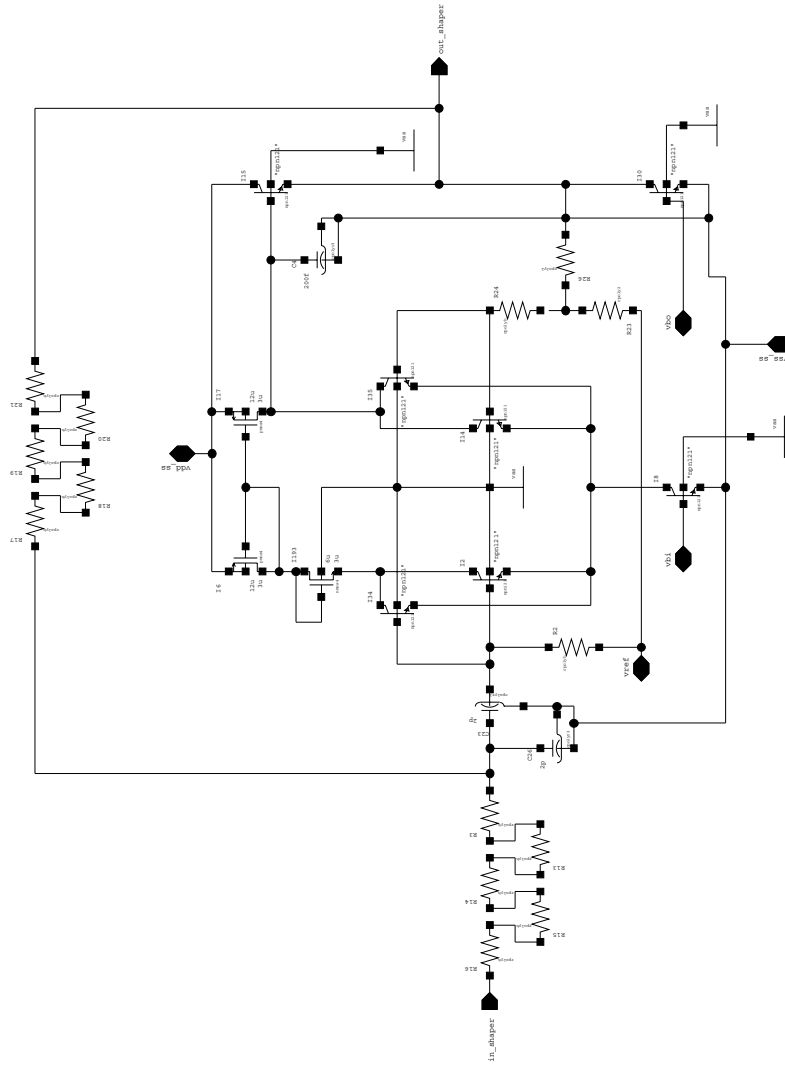


Figure C.27: Layout of the Slow Shaper designed in the mecano chip

D Version 2: Layout of the low impedance preamplifier

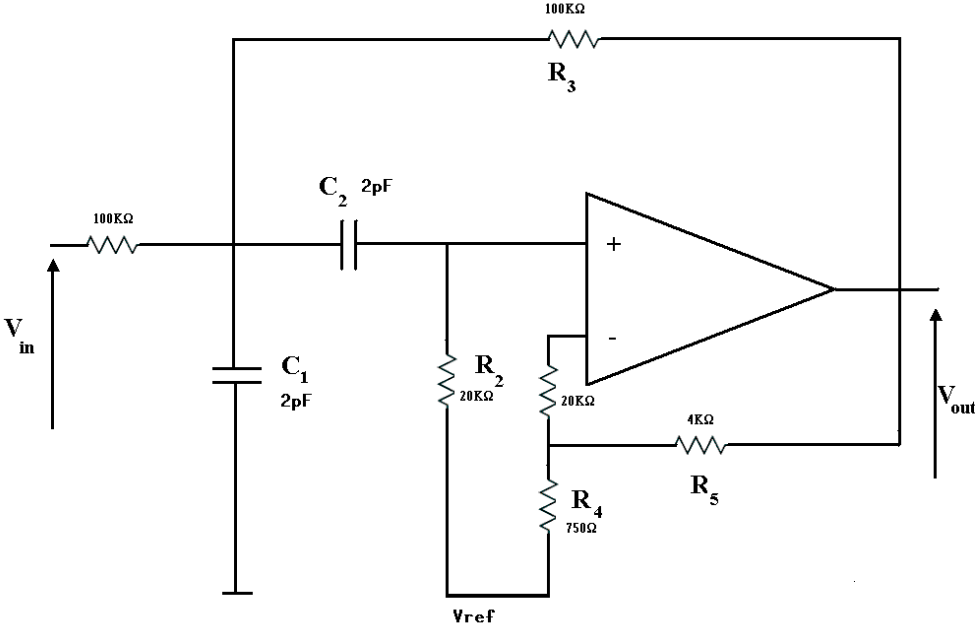


Figure D.28: *Layout of the Sallenkey low impedance preamp designed in Vers. 2*

E Version 2: Layout of the Track & Hold architecture

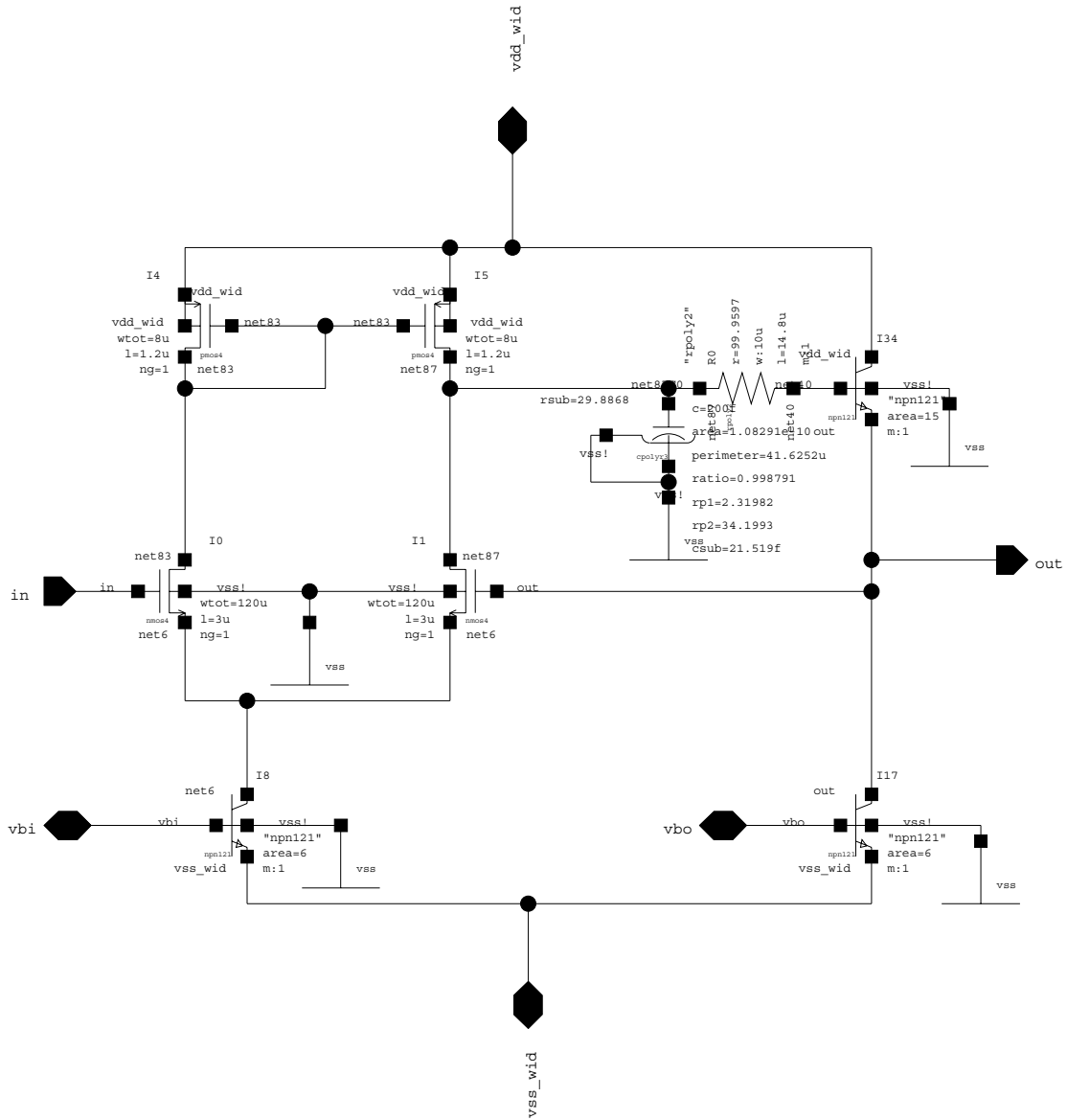


Figure E.29: Layout of the new Track & Hold architecture designed for Vers. 2

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